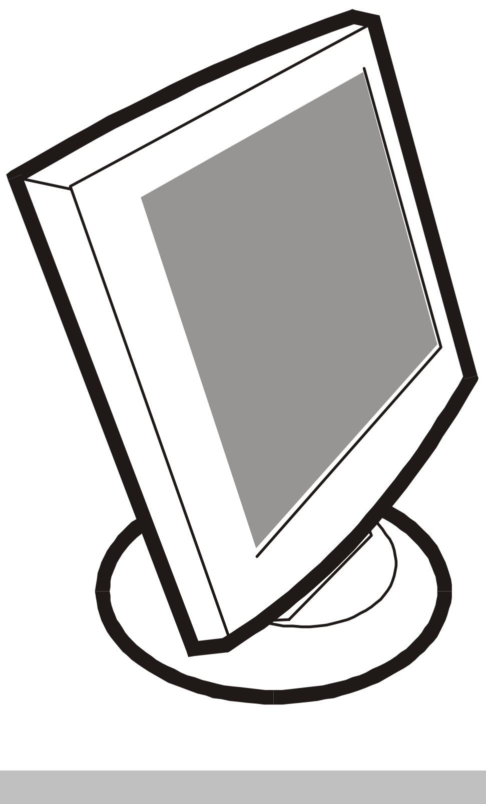
SERVICE MANUAL

TFT-5017/FP5017 LCD MONITOR
FOR COMPAQ



Ver: 00

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MANUFACTURE DATA: Jun 22 2002

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1. SPECIFICATIONS FOR LCD MONITOR

1-1 General specifications

1. LCD-PANEL :

Active display area	15 inches diagonal
Pixel pitch	0.297 mm x 0.297 mm
Pixel format	1024 x 768 RGB vertical stripe arrangement

2. Display Color :
   6-bit, 262144 colors

3. External Controls :
   Horizontal Position, Vertical Position, Clock, Clock Phase and Auto Adjustment
   Power On/Off, Brightness, Contrast, Color Select (6500°K, 9300°K, and Custom Color), Language Selection, OSD Controls and the functions included in the Management Menu.,

4. Input Video Signal :
   Analog-signal 0.7Vpp
   Video signal termination impedance 75 OHM

5. Scanning Frequencies :

Horizontal:	30 KHz - 61 KHz
Vertical:	56 Hz – 75 Hz
Pixel clock:	80 MHz

6. Factory Preset Timing : 11
   User Timings : 8
   Input signal tolerance : H tolerance ±0.5 K, V tolerance ±1 Hz

7. Power Source :
   Switching Mode Power Supply
   AC 90 – 265 V, 50/60 Hz Universal Type

8. Operating Temperature : 5℃ - 35℃ Ambient
   Non-operating Temperature : -20℃ - 60℃

9. Humidity :
   Operating : 20% to 80% RH (non-condensing)
   Non Operating : 5% to 90%RH (38.7℃ maximum wet bulb temperature)

10. Weight :
    5.8 kg
11. External Connection : 15Pin D-type Connector, AC power-Cord

12. View Angle : x-axis right/left = 60, y-axis up/down = 45

13. Outside dimension : Width x Height x Thickness = H:470 mm x W:183 mm x L:432 mm

14. Plug and Play : VESA DDC1/DDC2B

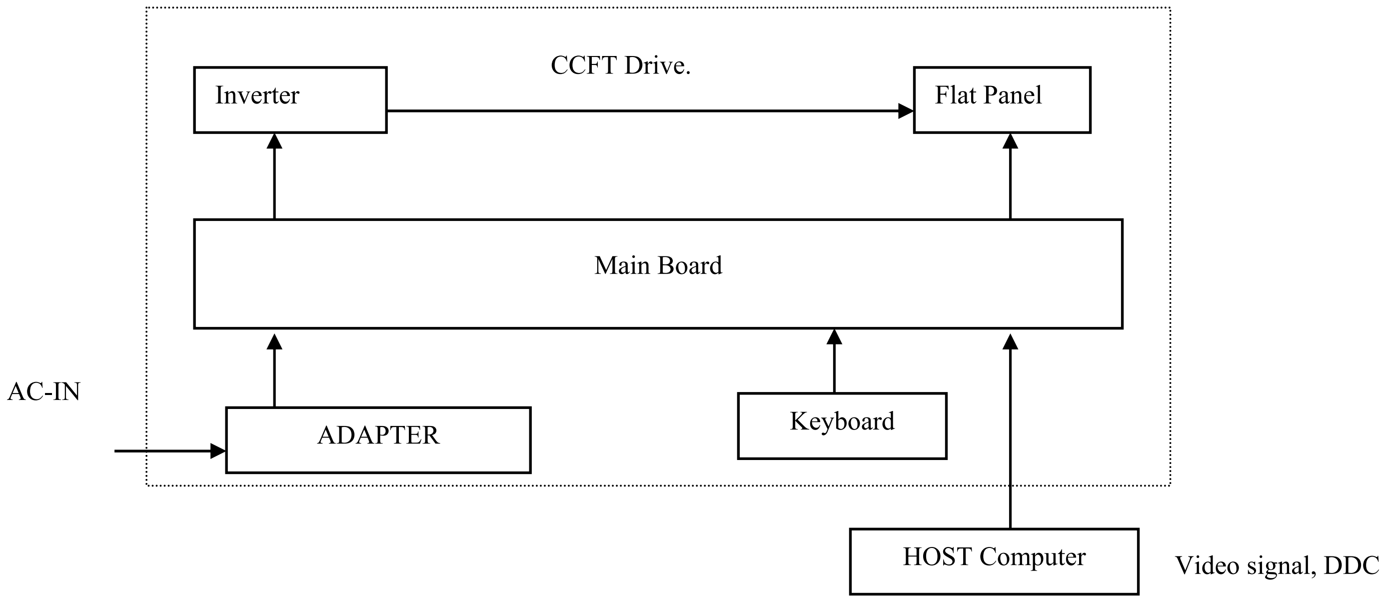
15. Power saving : VESA DPMS

1-2 LCD MONITOR DESCRIPTION

The LCD MONITOR will contain an main board, an inverter board, a power switch board and a keyboard. The main board will house the flat panel control logic, brightness control logic, DDC and DC-DC conversion to supply the appropriate power to the whole board and LCD panel, and transmitting TTL level signals into LCD Module to drive the LCD display circuit.

The inverter board will drive the two CCFLs (Cold Cathode Fluorescent Tube).
The switching power board will provides the power ON/OFF control over the whole monitor and control for DPMS LED indicator.
The function keyboard will provides the OSD control signal to the Main Board.

Monitor Block Diagram



1-3 Interface Connectors

(A) Power Cable
(B) Video Signal Connectors and Cable

2. PRECAUTIONS AND NOTICES

2-1 ASSEMBLY PRECAUTION

(1) Please do not press or scratch LCD panel surface with anything hard. And do not soil LCD panel surface by touching with bare hands (Polarizer film, surface of LCD panel is easy to be flawed)
In the LCD panel, the gap between two glass plates is kept perfectly even to maintain display characteristic and reliability. If this panel is subject to hard pressing, the following occurs :
(a) Uniform color (b) Orientation of liquid crystal becomes disorder
(2) Please wipe out LCD panel surface with absorbent cotton or soft cloth in case of it being soiled.
(3) Please wipe out drops of adhesive like saliva and water in LCD panel surface immediately.
They might damage to cause panel surface variation and color change.
(4) Do not apply any strong mechanical shock to the LCD panel.

2-2 OPERATING PRECAUTIONS

(1) Please be sure to unplug the power cord before remove the back-cover. (be sure the power is turn-off)
(2) Please do not change variable resistance settings in MAIN-BOARD, they are adjusted to the most suitable value. If they are changed, it might happen LUMINANCE does not satisfy the white balance spec.
(3) Please consider that LCD backlight takes longer time to become stable of radiation characteristic in low temperature than in room temperature.
(4) Please pay attention to displaying the same pattern for very long-time. Image might stick on LCD.

2-3 STORAGE PRECAUTIONS

(1) When you store LCD for a long time, it is recommended to keep the temperature between 0℃-40℃ without the exposure of sunlight and to keep the humidity less than 90% RH.
(2) Please do not leave the LCD in the environment of high humidity and high temperature such as 60℃ 90%RH.
(3) Please do not leave the LCD in the environment of low temperature; below -15℃.

2-4 HIGH VOLTAGE WARNING

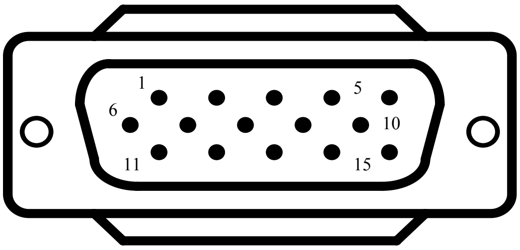
The high voltage was only generated by INVERTER module, if carelessly contacted the transformer on this module, can cause a serious shock. (the lamp voltage after stable around 600V, with lamp current around 8mA, and the lamp starting voltage was around 1500V, at Ta=25℃)

3. OPERATING INSTRUCTIONS

This procedure gives you instructions for installing and using the TFT5017/FP5017 LCD monitor display.

1. Position the display on the desired operation and plug the power cord into a convenient AC outlet. Three-wire power cord must be shielded and is provided as a safety precaution as it connects the chassis and cabinet to the electrical conduct ground. If the AC outlet in your location does not have provisions for the grounded type plug, the installer should attach the proper adapter to ensure a safe ground potential.

2. Connect the 15-pin color display shielded signal cable to your signal system device and lock both screws on the connector to ensure firm grounding. The connector information is as follow:



15 - Pin Color Display Signal Cable

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1.	RED	9.	5V power from VGA-card
2.	GREEN	10.	GND
3.	BLUE	11.	NC
4.	NC	12.	SDA
5.	GND	13.	HORIZ. SYNC
6.	GND-R	14.	VERT. SYNC
7.	GND-G	15.	SCL
8.	GND-B		

3. Apply power to the display by turning the power switch to the "ON" position and allow about thirty seconds for Panel warm-up. The Power-On indicator lights when the display is on.
4. With proper signals feed to the display, a pattern or data should appear on the screen, adjust the brightness and contrast to the most pleasing display, or press auto-key to get the best picture-quality.
5. This monitor has power saving function following the VESA DPMS. Be sure to connect the signal cable to the PC.
6. If your TFT5017/FP5017 LCD monitor requires service, it must be returned with the power cord.

4. ADJUSTMENT

4-1 ADJUSTMENT CONDITIONS AND PRECAUTIONS

1. Approximately 30 minutes should be allowed for warm up before proceeding.
2. Adjustments should be undertaken only on following function :Horizontal Position, Vertical Position, Clock, Clock Phase, Brightness, Contrast, Color Select (6500°K, 9300°K, and Custom Color)

4-2 ADJUSTMENT METHOD

Press MENU key to show OSD window or select function, and Left/Right key to switch the function controls or done the adjustment.



1. White-Balance, Luminance adjustment
   Before started adjust white balance ,lets setting the Chroma-7120 MEM. Channel 1 to 9300 color and MEM. channel 2 to 6500 color, how to setting MEM.channel you can reference to chroma 7120 user guide or simple use " SC" key and " NEXT" key to modify xyY value and use "ID" key to modify your own description

   Following is the step to do white-balance adjust

   Press MENU key and Right key for 2 seconds at power on (replug power cord) will be in factory mode.

   I. Bias (Low luminance) adjustment :

   Wait for message " Pass" appear then adjust OSD contrast and brightness to "90".

   II. Gain (High light) adjustment :

   a. adjust 9300 color-temperature

   change chroma-7120 to channel 1,Switch the chroma-7120 to RGB-mode(with press "MODE") ,and selected OSD item "F" (at OSD right down corner), Enter AOC Compaq1 Menu

   The lcd-indicator will show x = 281 ±10, y = 311 ±10, Y = 230 ±5 cd/m^2

   Adjust 9300k RGB until R=100, G=100, B=100, and then switch the chroma-7120 to xyY mode

   (With press "MODE")

   b. adjust 6500 color-temperature

   change chroma-7120 to channel 2, Switch the chroma-7120 to RGB-mode(with press "MODE"),

   The lcd-indicator will show x = 313 ±10, y = 329 ±10, Y = 230 ±5 cd/m^2

   Adjust 6500k RGB until R=100, G=100, B=100, and then switch the chroma-7120 to xyY mode

   (With press "MODE")

   Press POWER-key off-on to quit from factory mode (in USER-mode, the OSD location was placed at middle of screen)

2. Clock adjustment
   Set the Chroma at pattern 63 (cross-talk pattern) or WIN98/95 shut-down mode (dot-pattern).
   Adjust until the vertical-shadow as wide as possible or no visible.
   This function is adjust the PLL divider of ADC to generate an accurate pixel clock
   Example : Hsyn = 31.5KHz Pixel freq. = 25.175MHz (from VESA spec)
   The Divider number is (N) = (Pixel freq. x 1000)/Hsyn
   From this formula, we get the Divider number, if we fill this number in ADC register (divider register), the PLL of ADC will generate a clock which have same period with above Pixel freq.(25.175MHz) the accuracy of this clock will effect the size of screen.(this clock was called PIXEL-CLOCK)

3. Phase adjustment
   Set the Chroma at pattern 63 (cross talk pattern) or WIN98/95 shut down mode (dot-pattern).
   Adjust the horizontal interference as less as possible
   This function is adjust the phase shift of PIXEL-CLOCK to acquire the right pixel data .
   If the relationship of pixel data and pixel clock not so match, we can see the horizontal interference at screen only at crosstalk pattern and dot pattern we can find this phenomena, other pattern the affect is very light

4. H/V-Position adjustment
   Set the Chroma at pattern 1 (crosshatch pattern) or WIN98/95 full-white pattern confirm above 2 functions (clock & focus) was done well, if that 2 functions failed, the H/V position will be failed too.
   Adjust the four edge until all four-edges are visible at the edge of screen.

5. MULTI-LANGUAGE function
   There have 6 language for selection, press "MENU" to selected and confirm , press " LEFT" or " RIGHT" to change the kind of language.

6. Reset function
   Clear each old status of auto-configuration and re-do auto-configuration (for all mode)
   This function also recall 6500 color-temperature , if the monitor status was in " Factory-mode" this reset function will clear Power-on counter too.

7. OSD-LOCK function
   The OSD functionality shall be enabled or disabled by pressing the "menu" button and holding it for 10 seconds. Upon disabling the OSD, an OSD message of "OSD Lockout" shall be displayed for 10 seconds. When the OSD is locked and any OSD button is pressed, the OSD message "OSD Locked" shall be displayed for an additional 10 seconds. When the OSD is locked, holding the OSD button for 10 seconds will unlock the OSD and display the main menu.

8. View Hours Total Operation and Hours Backlight On (if not necessary , not suggest to entry Service Mode,it is entered by pressing the power switch while the **menu** button is held in.)
   Total Hours track and record the total hours that it has been powered up. This value shall be stored in the system memory. The Hours Total Operation shall be incremented 31 minutes after power is applied, and once each hour after that while power is still active.
   Backlight Hours track and record the number of hours the backlight tubes have had power applied to them. This shall be independent of the brightness or contrast controls. The Hours Backlight On shall be incremented 31 minutes after power has been continuously applied to the backlight, and once each hour after that while power is still applied to the backlight.
   The Backlight Hours was used to record how long the backlight of panel already working, the backlight life time was guarantee minimal 30000 hours, the maintainer can check the record only in Service Mode. pressing the power switch while the **menu** button is held in will be in f service mode.
   "Reset Total Hours " clear the powered up counter to zero hours.
   "Reset Backlight Hours " clear Backlight Hours counter to zero hours.

4-3 MAIN ADJUSTMENTS

Power Key : Press to turn on or off the monitor.
Left Key : Press to perform automatic calculated CLOCK, PHASE, H/V POSITION, but no affect the color-temperature
Left/Right Key : press to perform select function or adjustment.
MENU Key : press to show the OSD menu at the monitor or to confirm your function selection

5. CIRCUIT-DESCRIPTION

5-1 SPECIAL FUNCTION with PRESS-KEY

Press MENU key and Right key, at POWER-ON: set to FACTORY-mode, when we want to adjust white-balance with rs232-port.
Press POWER-key off-on : CANCEL above function(quit from factory mode) and set to user-mode.
Press MENU key 10seconds : Enable/ Disable OSD-LOCK function

OSD-INDEX EXPLANATION

1. CABLE NOT CONNECTED :Check video cable.
2. INPUT NOT SUPPORT :
   a. INPUT frequency out of range : H > 61kHz, v > 75Hz or H < 30kHz, v < 56Hz
   b. INPUT frequency out of VESA-spec. (out of tolerance too far)
3. UNSUPPORT mode, try different Video-card Setting :
   Input frequency out of tolerance, but still can catch-up by our system (if this message show, that means, this is new-user mode, AUTO-CONFIG will disable)

5-2 SIMPLE-INTRODUCTION about TFT5017/FP5017 chipset

1. GM2115 (Genesis all-in-one solution for ADC, OSD,MCU,TCON,scalar and interpolation) :
   USE for computer graphics images to convert analog RGB data to digital data for interpolation process, zooming, OSD font & overlay and generate drive-timing for LCD-PANEL,

2. W49F002 (Winbond flash memory, with 64k Rom-size) :
   Use for store firmware, the firmware include calculate frequency, pixel-dot , detect change mode, rs232-communication, power-consumption control, OSD-index warning…etc.

3. M24C02 (MicroChip IC) :
   EePROM type, 1K ROM-SIZE, for saving DDC-CONTENT.

4. M24C16 (MicroChip IC) :
   EePROM type, 4K ROM-SIZE, for saving AUTO-config data, White-balance data, and Power-key status, backliaht on-counter data and power up –counter data.

5. BA9741F (swintching regulator 12V to 5V and 12V to 3.3V) :

6. RT9164-25CG (RICH TEK brand regulator 5V to 2.5V)

MODULE-TPYE COMPONENT :

1. ADAPTER : CONVERSION-module to convert AC 90V-265V to 12VDC, with 3.33 AMP

2. INVERTER : CONVERSION-module to convert DC 12V to High-Voltage around 1600V, with frequency 30K-50Khz, 7mA-10mA

6. Trouble-Shooting

****Use the PC Win 2000/98/95 white pattern, with some icon on it, and Change the Resolution to 640x480 60 Hz / 31 KHz**

I. NO SCREEN APPEAR

Check Adapter module have 12V output?

↓ YES

Check FPC cable loose or tight ?

↓ YES

Check Inverter Block Trouble shooting

↓ ok

Check Dc to Dc block trouble shooting → If the product name of this monitor is T563KCDHKCCPA or T563KCDHKCCPN Check Dc to Dc Module block trouble shooting

↓ ok

Check Scalar Trouble shooting

↓ ok

End

INVERTER BLOCK TROUBLE SHOOTING

Check the CN6 : Pin 1& Pin2 = 12v for Inverter power supply
CN6 : Pin 4 = Lamp current control → must have 0 volt to 3.3 volt Voltage variable when adjust Brightness
CN6 : Pin 6 = Inverter on-off control → must have 3.3volt when power switch on (LED green) and must have 0 volt When power switch off (LED orange)
Check all above status is meet or not ?

↓ no

Replace Inverter module to new one

DC to DC block trouble shooting

Check CN12 have 12v input ?

↓ yes

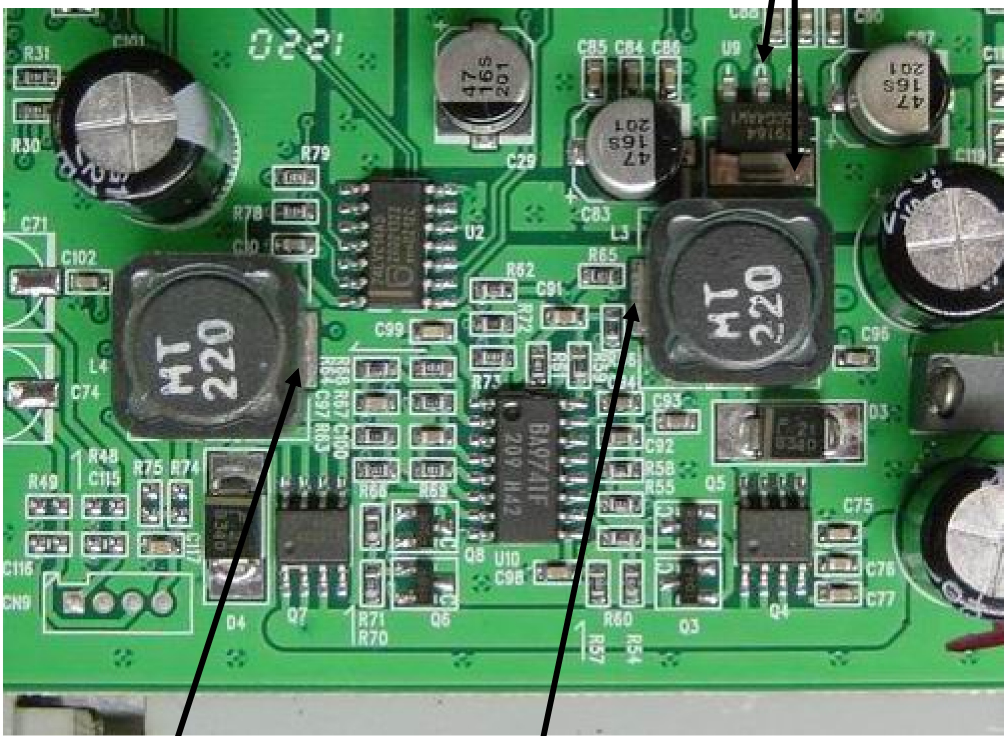
CHECK L3 have 3.3V output & L4 have 5V output?
U9 Pin2 have 2.5V output

→ no → Replace relative component

↓

End

U9 pin 2 = 2.5V



L4 pin 1 = 5V

L3 pin 1 = 3.3V

DC to DC Module block trouble shooting

Check U11Pin2 or Pin3 have 5V input ?

↓ yes

Check U11Pin4 have 3.3V input ? (when power on)
Check U11Pin4 have 0V input ? (when power off)

→ no: Replace Dc to Dc Module (U11) component

↓ yes

Check U11Pin7 have 9V output ?

→ no: Replace Dc to Dc Module (U11) component

↓ yes

Check U11Pin9 have -6V output ?

→ no: Replace Dc to Dc Module (U11) component

↓ yes

Check U11Pin12 have 3.6V output ?

→ no: Replace Dc to Dc Module (U11) component

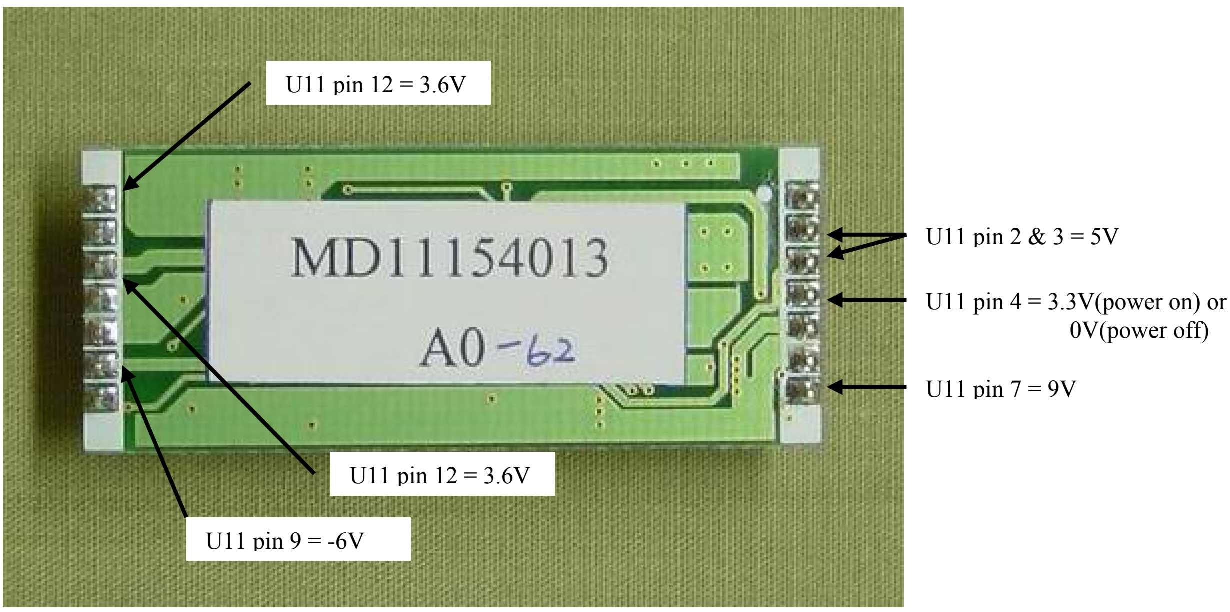
↓ yes

Check U11Pin14 have 18V output ?

→ no: Replace Dc to Dc Module (U11) component

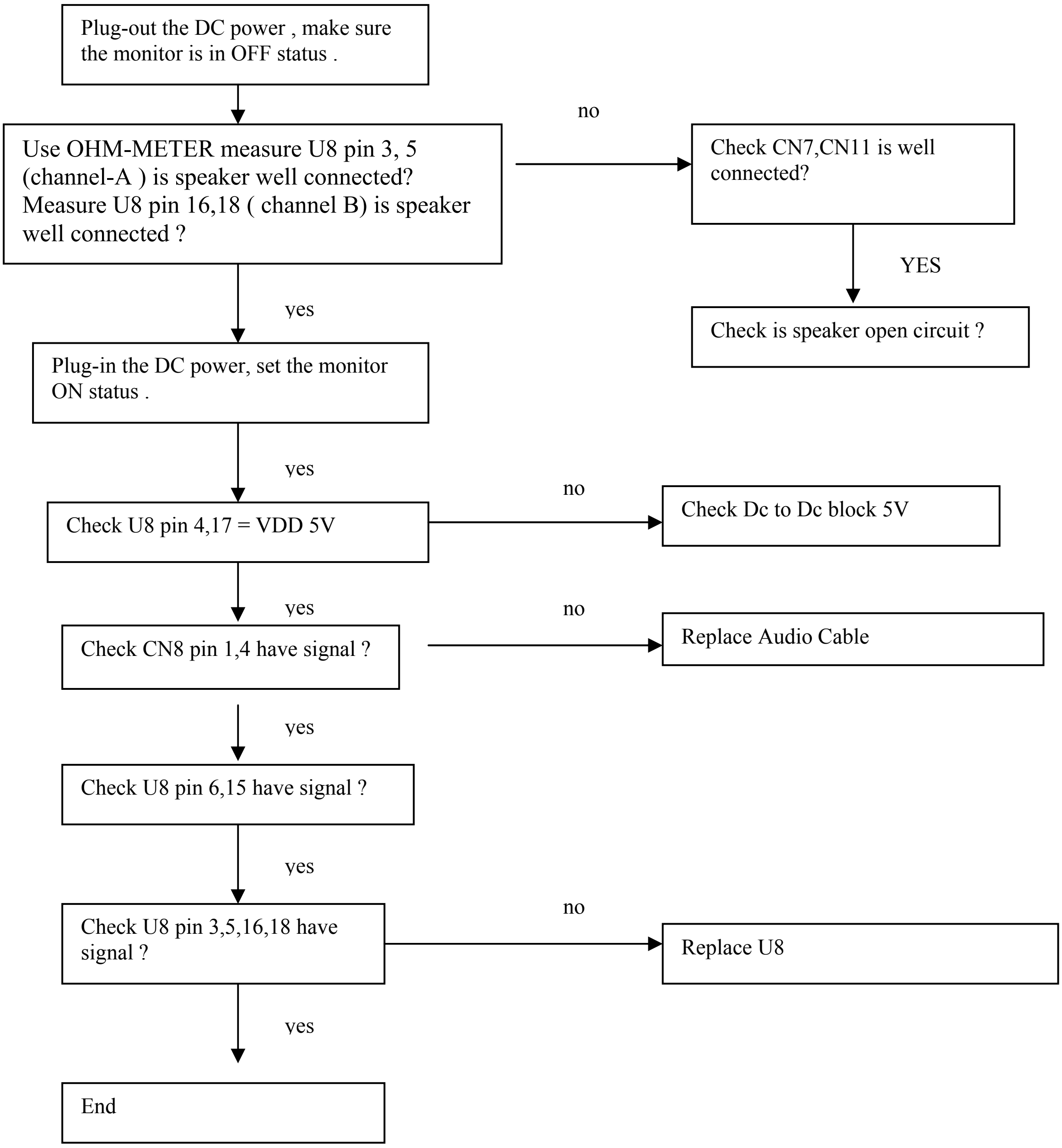
↓ yes

End

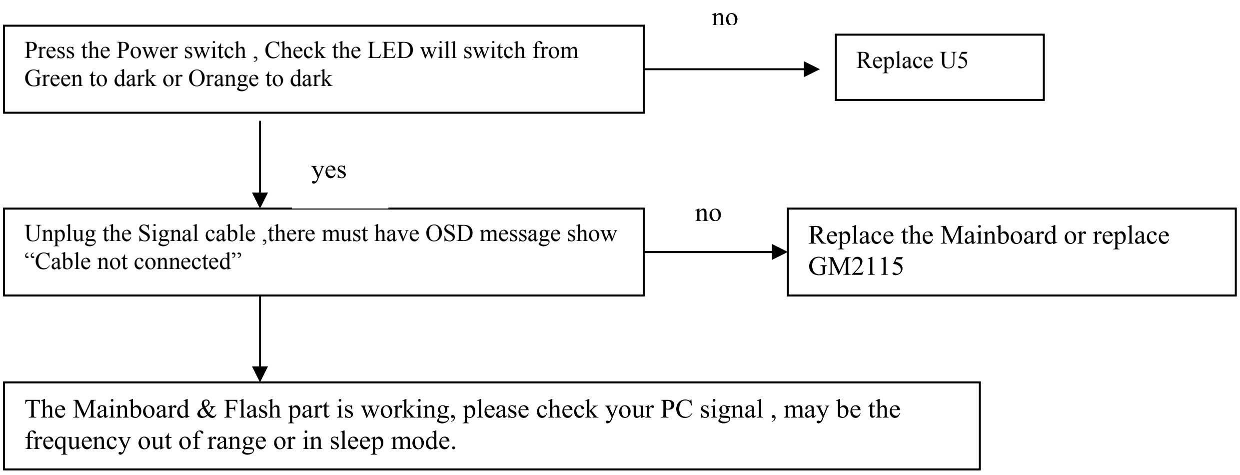


<u>AUDIO-MODULE Trouble shooting chart</u>

NO VOICE OUTPUT

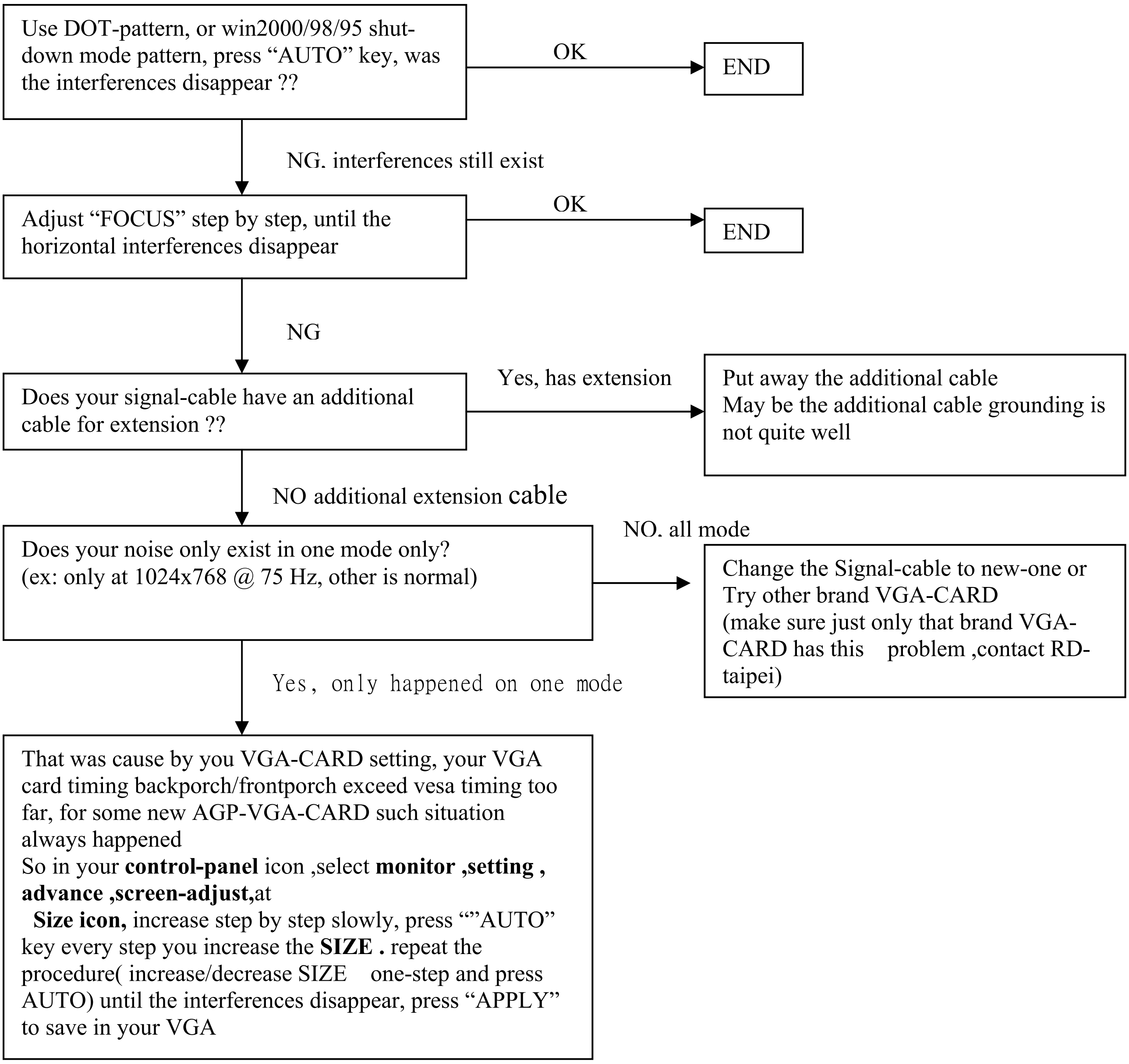


Scalar BLOCK TROUBLE SHOOTING



II.ALL SCREEN HAS INTERFERENCES OR NOISE, CAN'T BE FIXED BY AUTO KEY

**** NOTE:** There is so many kind of interferences, 1). One is cause by some VGA-CARD that not meet VESA spec or power grounding too bad that influence our circuit
2).other is cause by external interferences, move the monitor far from electronic equipment.(rarely happened)



III. DOS MODE has jitter

NOTE :the rule of doing AUTO-CONFIGURATION : must be a full-size screen, if the screen not full , the auto-configuration will fail. So in dos mode ,just set your “CLOCK” in OSD-MENU to zero or use some full screen edit file (ex: PE2, HE) and press “AUTO”

Ⅳ. THERE WAS SNOW PHENOMENA or BRIGHT NOISE ON THE SCREEN

When use pattern 32 Gray-scale / or 16 Gray scale, there is a **snow phenomena on the screen (like a noise spread** inside) that means data missing, may be cause by FPC loose, or resistor array cold-solder

Check the FPC loose or tight or Replace a new FPC

↓

Re solder all resistor array from LP1 – LP13

↓

Replace Mainboard to new one

Ⅴ. THE PANEL LUMINANCE WAS DOWN

Set Contrast & brightness =maximal, RGB= 50
Quit from OSD-screen, measured Y(luminance)
With chroma 7120, check Y= 250±10 CD/M2 ?

OK →

If Y can reach ＞230 cd/m2 that means
The lamp still working well, so we just re-do the white-balance process
Please refer to page 7

NG ↓

If the Y less than 160 cd/m2 (after the Brightness & contrast = max) then change the LAMP of panel

PRELIMINARY DATA SHEET

gm5115/25

XGA/SXGA OnPanel LCD Panel Controller

*** Genesis Microchip Confidential ***

C5115-DAT-01E

August 2001

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Revision History

Document	Description	Date
C5115-DAT-01A	• Initial release.	March 2001
C5115-DAT-01B	• In Table 18 corrected description of OSC_SEL (on pin ROM_ADDR13). It should be set to 1 to indicate usage of a single-ended clock oscillator. • Corrected image and orientation of logo in pinout diagram Figure 2. • Added section 4.11.3.	June 2001
C5115-DAT-01C	• Replaced all occurrences of CVDD with CVDD_2.5, including pin numbers 26, 88, 134 and 203 to make them consistent with the names of other 2.5V voltage supply signals.	July 2001
C5115-DAT-01D	• Pin number 205 name changed from GPIO16/HFS to GPIO16/HFSn and all occurrences of HFS replaced with HFSn to reflect the fact that this signal is active low. • Added description of 2-wire serial protocol in section 4.16.2 and Table 24. • Removed "Read with Increment" operation description. • Corrected mechanical specification in Figure 32. • Changes to Table 21 – DC Characteristics: - Maximum voltage for 5V-tolerance inputs is 5.5V. - Added maximum current requirements. • Added description of OCM Standalone configuration Figure 25. • Added Figure 21 – Panel Power Sequencing.	July 2001
C5115-DAT-01E	• Added description of gm5125 (SXGA device). • Pin names changed to reflect alternate hard-wired functions: - pin 50 from GPIO11 to GPIO11/ROM_WEn, - pin 51 from GPIO12 to GPIO12/NVRAM_SDA, - pin 52 from GPIO13 to GPIO13/NVRAM_SCL, - pin 6 from DDC_SCL to GPIO14/DDC_SCL, - pin 7 from DDC_SDA to GPIO15/DDC_SDA, - pin 46 from GPIO6 to GPIO6/TCON_SHC, - pin 47 from GPIO7 to GPIO7/TCON_TDIV. • Removed description of 6-wire host interface, since this is not recommended operation. Pin 1 name changed from GPIO17/HDATA0 to GPIO17, and similarly for pins 206, 207 and 208. • Corrected maximum ADC sampling frequency in Table 15 and maximum ADC_CLK frequency in Table 22 to 162.5MHz. • Added section 4.5 Test Pattern Generator. • Added description of TCON_SHC and TCON_TDIV in section 4.12.1. • Clarifications to section 4.1 describing clock generation, section 4.7.2 describing sRGB support, and section 4.14.3 describing GPIOs. • Removed mention of row attributes in Figure 24. gm5115/25 OSD controller does not have row attributes. • Corrected Table 21, Note 3. Pins VDD1_ADC_2.5, VDD2_ADC_2.5, VDD_RX0_2.5, VDD_RX1_2.5 and VDD_RX2_2.5 are digital 2.5V supplies, not analog. • Changed signal names SCL and SDA to HCLK and HFSn, respectively in Figure 29, Figure 30, and Figure 31.	August 2001

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1. OVERVIEW

The gm5115/25 is a graphics processing IC for Liquid Crystal Display (LCD) monitors at XGA/SXGA resolution. It provides all key IC functions required for image capture, processing and timing control for direct interface to the row and column drivers of the LCD panel. On-chip functions include a high-speed triple-ADC and PLL, Ultra-Reliable DVI ™ receiver, a high quality zoom and shrink scaling engine, an on-screen display (OSD) controller, an on-chip microcontroller (OCM), and a programmable panel timing controller (TCON). With all these functions integrated onto a single device, the gm5115/25 eliminates the need for a printed circuit board (PCB) from the system along with the associated connectors and cables. Therefore, the gm5115/25 simplifies the design and reduces the cost of LCD monitors while maintaining a high-degree of flexibility and quality.

1.1 gm5115/25 System Design Example

Figure 1 below shows a typical dual interface LCD monitor system based on the gm5115/25. Designs based on the gm5115/25 have reduced system cost, simplified hardware and firmware design and increased reliability because only a minimal number of components are required in the system.

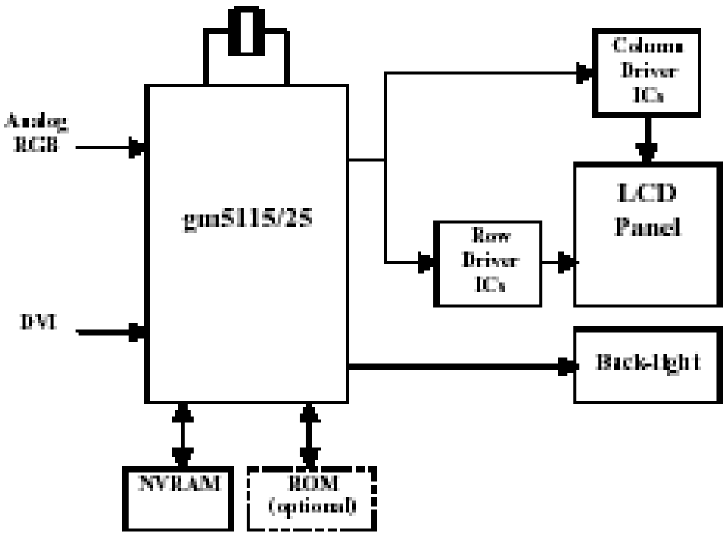


Figure 1.   gm5115/25 System Design Example

1.2 gm5115/25 Features

FEATURES

- Zoom (from VGA) and shrink (from UXGA) scaling
- Integrated 8-bit triple-channel ADC / PLL
- Integrated Ultra-Reliable DVI 1.0-compliant receiver
- High-Bandwidth Digital Content Protection (HDCP)
- On-chip programmable OnPanel timing controller
- Embedded microcontroller with parallel ROM interface
- On-chip versatile OSD engine
- All system clocks synthesized from a single external crystal
- Programmable gamma correction (CLUT)
- RealColor controls provide sRGB compliance
- PWM back light intensity control
- 5 Volt tolerant inputs
- Low EMI and power saving features

- **High-Quality Advanced Scaling**
  - Fully programmable zoom ratios
  - High-quality shrink capability from UXGA resolution
  - RealRecovery/TM function provides full color recovery image for refresh rates higher than those supported by the LCD panel
  - Moire cancellation

- **Analog RGB Input Port**
  - Supports up to 162.5MHz (SXGA 75Hz / UXGA 60Hz)
  - On-chip high-performance PLLs (only a single reference crystal required)

- **Auto-Configuration / Auto-Detection**
  - Input format detection
  - Phase and image positioning

- **Ultra-Reliable DVI Compliant Input Port**
  - Operating up to 165MHz (up to UXGA 60Hz)
  - Direct connect to all DVI compliant digital transmitters
  - High-bandwidth Digital Content Protection (HDCP)

- **RealColor™ Technology**
  - Digital brightness and contrast controls
  - TV color controls including hue and saturation controls
  - Flesh-tone adjustment
  - Full color matrix allows end-users to experience the same colors as viewed on CRTs and other displays (e.g. sRGB compliance)

- **On-chip OSD Controller**
  - On-chip RAM for downloadable menus
  - 1, 2 and 4-bit per pixel character cells
  - Horizontal and vertical stretch of OSD menus
  - Blinking, transparency and blending

- **On-chip Microcontroller**
  - Requires no external micro-controller
  - External parallel ROM interface allows firmware customization with little additional cost
  - 23 general-purpose inputs/outputs (GPIOs) available for managing system devices (keypad, back-light, NVRAM, etc)
  - Industry-standard firmware embedded on-chip, requires no external ROM (configuration settings stored in NVRAM)

- **Built-in OnPanel Timing Controller**
  - Eliminates the need for an external panel timing controller (TCON) device, thereby reducing system cost
  - Direct connect to commercial row/column driver ICs (supports dual-bus / dual-port and dual-bus / single-port)
  - Low EMI and power saving features include frame, line and in-line inversion, blanking, data staggering and slew rate control.

- **Programmable Output Format**
  - Single / double wide up to XGA/SXGA 75Hz output
  - Pin swap, odd / even swap and red / blue group swap of RGB outputs for flexibility in board layout
  - Support for 8 or 6-bit panels (with high-quality dithering)

- **Highly Integrated System-on-a-Chip Reduces Component Count for *Highly Cost Effective Solution***

- ***Standalone* operation requires no external ROM and no firmware development for *Fast Time to Market***

- **Pin and register compatible *OnPanel Family*:**
  - **gm5115/gm5125** Dual-Interface XGA/SXGA
  - **gm3115/gm3125** Digital-Interface XGA/SXGA
  - **gm2115/gm2125** Analog-Interface XGA/SXGA

2. GM5115/25 PINOUT

The gm5115/25 is available in a 208-pin Plastic Quad Flat Pack (PQFP) package. Figure 2 provides the pin locations for all signals.

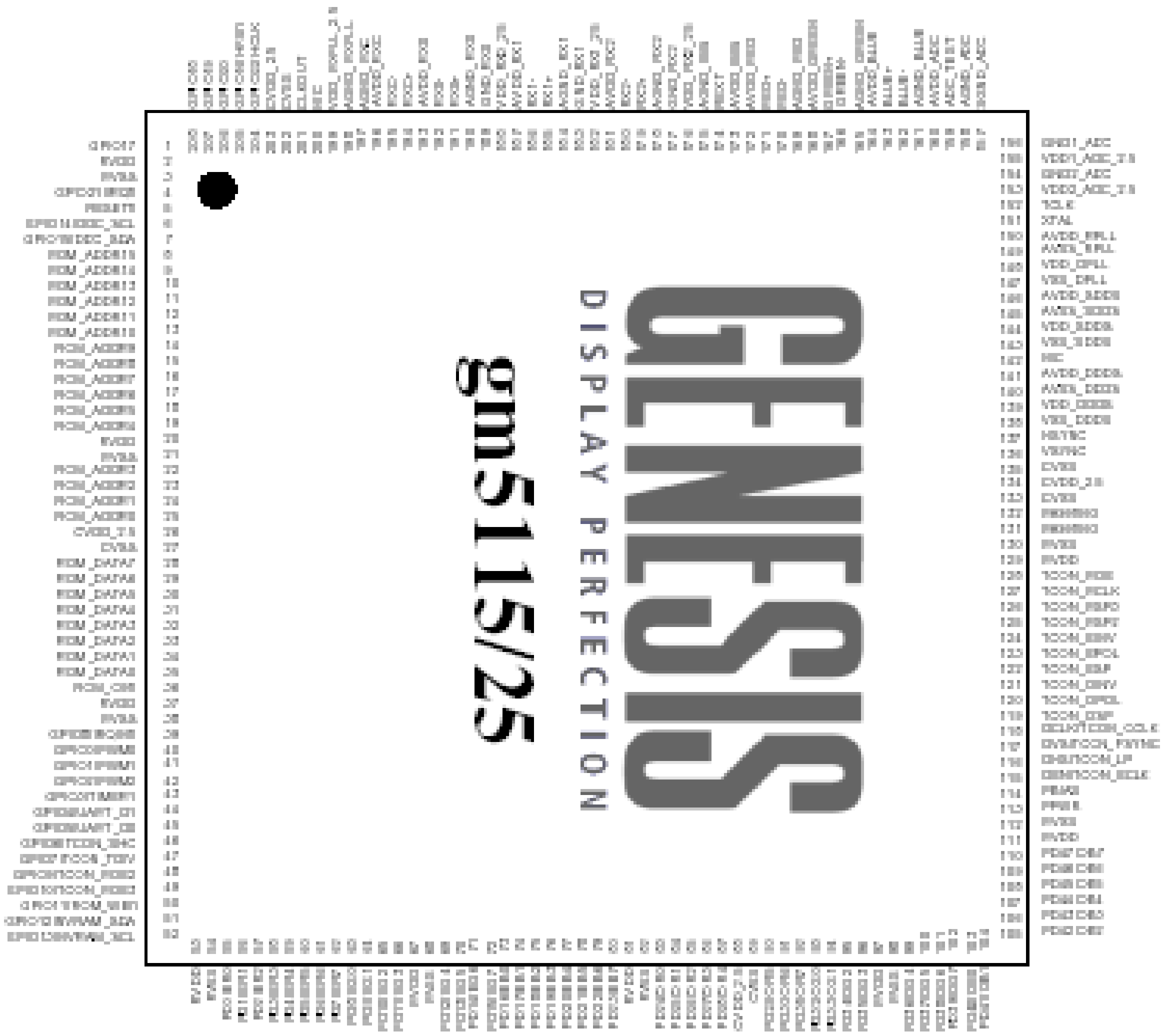


Figure 2. gm5115/25 Pin Out Diagram

3. GM5115/25 PIN LIST

I/O Legend: A = Analog, I = Input, O = Output, P = Power, G= Ground

Table 1. Analog Input Port

Pin Name	No.	I/O	Description
AVDD_RED	172	AP	Analog power (3.3V) for the red channel. Must be bypassed with decoupling capacitor to AGND_RED pin on system board (as close as possible to the pin).
RED+	171	AI	Positive analog input for Red channel.
RED-	170	AI	Negative analog input for Red channel.
AGND_RED	169	AG	Analog ground for the red channel. Must be directly connected to the analog system ground plane.
AVDD_GREEN	168	AP	Analog power (3.3V) for the green channel. Must be bypassed with decoupling capacitor to AGND_GREEN pin on system board (as close as possible to the pin).
GREEN+	167	AI	Positive analog input for Green channel.
GREEN-	166	AI	Negative analog input for Green channel.
AGND_GREEN	165	AG	Analog ground for the green channel. Must be directly connected to the analog system ground plane.
AVDD_BLUE	164	AP	Analog power (3.3V) for the blue channel. Must be bypassed with decoupling capacitor to AGND_BLUE pin on system board (as close as possible to the pin).
BLUE+	163	AI	Positive analog input for Blue channel.
BLUE-	162	AI	Negative analog input for Blue channel.
AGND_BLUE	161	AG	Analog ground for the blue channel. Must be directly connected to the analog system ground plane.
AVDD_ADC	160	AP	Analog power (3.3V) for ADC analog blocks that are shared by all three channels. Includes band gap reference, master biasing and full-scale adjust. Must be bypassed with decoupling capacitor to AGND_ADC pin on system board (as close as possible to the pin).
ADC_TEST	159	AO	Analog test output for ADC. Do not connect.
AGND_ADC	158	AG	Analog ground for ADC analog blocks that are shared by all three channels. Includes band gap reference, master biasing and full-scale adjust. Must be directly connected to analog system ground plane.
SGND_ADC	157	AG	Dedicated pad for substrate guard ring that protects the ADC reference system. Must be directly connected to the analog system ground plane.
GND1_ADC	156	G	Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
VDD1_ADC_2.5	155	P	Digital power (2.5V) for ADC encoding logic. Must be bypassed with decoupling capacitor to GND1_ADC pin on system board (as close as possible to the pin).
GND2_ADC	154	G	Digital GND for ADC clocking circuit. Must be directly connected to the digital system ground plane.
VDD2_ADC_2.5	153	P	Digital power (2.5V) for ADC encoding logic. Must be bypassed with decoupling capacitor to GND2_ADC pin on system board (as close as possible to the pin).
HSYNC	137	I	ADC input horizontal sync input. [Input, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
VSYNC	136	I	ADC input vertical sync input. [Input, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]

Table 2. DVI Input Port

Pin Name	No	I/O	Description
AVDD_IMB	173	AP	Analog VDD (3.3V) for internal biasing circuits. Must be bypassed with decoupling capacitors (as close as possible to the pin).
REXT	174	AI	External reference resistor. An external 1Kohm (1%) resistor should be connected from this pin to AVDD_IMB pin.
AGND_IMB	175	AG	Analog GND for internal biasing circuits. Must be connected directly to the ground plane.
VDD_RX2_2.5	176	P	VDD (2.5V) for TMDS input pair 2 logic circuits. Must be bypassed with decoupling capacitor to GND_RX2 pin (as close as possible to the pin).
GND_RX2	177	G	GND for TMDS input pair 2 logic circuits. Must be connected directly to the ground plane.
AGND_RX2	178	AG	Analog GND for TMDS input pair 2 input buffer. Must be connected directly to the analog ground plane.
RX2+	179	AI	TMDS input pair 2
RX2-	180	AI	TMDS input pair 2
AVDD_RX2	181	AP	Analog VDD (3.3V) for TMDS input pair 2 input buffer. Must be bypassed with decoupling capacitor to AGND_RX2 pin (as close as possible to the pin).
VDD_RX1_2.5	182	P	VDD (2.5V) for TMDS input pair 1 logic circuits. Must be bypassed with decoupling capacitor to GND_RX1 pin (as close as possible to the pin).
GND_RX1	183	G	GND for TMDS input pair 1 input buffer. Must be connected directly to the analog ground plane.
AGND_RX1	184	AG	Analog GND for TMDS input pair 1 input buffer. Must be connected directly to the analog ground plane.
RX1+	185	AI	TMDS input pair 1
RX1-	186	AI	TMDS input pair 1
AVDD_RX1	187	AP	Analog VDD (3.3V) for TMDS input pair 1 input buffer. Must be bypassed with decoupling capacitor to AGND_RX1 pin (as close as possible to the pin).
VDD_RX0_2.5	188	P	VDD (2.5V) for TMDS input pair 0 logic circuits. Must be bypassed with decoupling capacitor to GND_RX0 pin (as close as possible to the pin).
GND_RX0	189	G	GND for TMDS input pair 0 logic circuits. Must be connected directly to the ground plane.
AGND_RX0	190	AG	Analog GND for TMDS input pair 0 input buffer. Must be connected directly to the analog ground plane.
RX0+	191	AI	TMDS input pair 0
RX0-	192	AI	TMDS input pair 0
AVDD_RX0	193	AP	Analog VDD (3.3V) for TMDS input pair 0 input buffer. Must be bypassed with decoupling capacitor to AGND_RX0 pin (as close as possible to the pin).
RXC+	194	AI	TMDS input clock pair
RXC-	195	AI	TMDS input clock pair
AVDD_RXC	196	AP	Analog VDD (3.3V) for TMDS input clock pair input buffer. Must be bypassed with 100pF capacitor to AGND_RXC pin (as close as possible to the pin).
AGND_RXC	197	AG	Analog GND for TMDS input clock pair input buffer. Must be connected directly to the analog ground plane.
GND_RXPLL	198	G	Digital GND for the TMDS receiver internal PLL. Must be connected directly to the system ground plane.
VDD_RXPLL_2.5	199	AP	Analog VDD (2.5V) for the TMDS receiver internal PLL. Must be bypassed with a decoupling capacitor to AGND_RXPLL pin (as close as possible to the pin).
CLKOUT	201	AO	For test purposes only. Do not connect.

Table 3. RCLK PLL Pins

Pin Name	No	I/O	Description
AVDD_RPLL	150	AP	Analog power for the Reference DDS PLL. Connect to 3.3V supply. Must be bypassed with a 0.1uF capacitor to pin AVSS_RPLL (as close to the pin as possible).
AVSS_RPLL	149	AG	Analog ground for the Reference DDS PLL. Must be directly connected to the analog system ground plane.
TCLK	152	AI	Reference clock (TCLK) from the 14.3MHz crystal oscillator (see Figure 4), or from single-ended CMOS/TTL clock oscillator (see Figure 7). This is a 5V-tolerant input. See Table 14.
XTAL	151	AO	Crystal oscillator output.
VDD_DPLL	148	P	Digital power for FCLK and RCLK PLLs. Connect to 3.3V supply.
VSS_DPLL	147	G	Digital ground for FCLK and RCLK PLLs.

Table 4. System Interface and GPIO Signals

Pin Name	No	I/O	Description
RESETn	5	I	Active-low hardware reset signal. The reset signal must be held low for at least 1µS. [Input, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO0/PWM0	40	IO	General-purpose input/output signal or PWM0. Open drain option via register setting. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO1/PWM1	41	IO	General-purpose input/output signal or PWM1. Open drain option via register setting. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO2/PWM2	42	IO	General-purpose input/output signal or PWM2. Open drain option via register setting. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO3/TIMER1	43	IO	General-purpose input/output signal. Open drain option via register setting. This pin is also connected to Timer 1 clock input of the OCM. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO4/UART_DI	44	IO	General-purpose input/output signal. Open drain option via register setting. This pin is also connected to the OCM UART data input signal by programming an OCM register. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO5/UART_DO	45	IO	General-purpose input/output signal. Open drain option via register setting. This pin is also connected to the OCM UART data output signal by programming an OCM register. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO6/TCON_SHC	46	IO	General-purpose input/output signal. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO7/TCON_TDIV	47	IO	General-purpose input/output signal. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO8/IRQINn	39	IO	General-purpose input/output signal. This is also active-low interrupt input to OCM and is directly wired to OCM int_0n. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO9/TCON_ROE2	48	IO	General-purpose input/output signal. Open drain option via register setting. This pin can also function as TCON signal ROE2. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO10/TCON_ROE3	49	IO	General-purpose input/output signal. Open drain option via register setting. This pin can also function as TCON signal ROE3. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO11/ROM_WEn	50	IO	General-purpose input/output signal, or ROM write enable if a programmable FLASH device is used. Open drain option via register setting. [Bi-directional Input, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO12/NVRAM_SDA GPIO13/NVRAM_SCL	51 52	IO IO	General-purpose input/output signals, or 2-wire master serial interface to NVRAM in standalone mode. Open drain option via register setting. [Bi-directional Input, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO14/DDC_SCL GPIO15/DDC_SDA	6 7	IO IO	DDC Interface for DVI-HDCP communication. This is 5V-tolerant SCL pin.
GPIO16/HFSn	205	IO	General-purpose input/output signal when host port is disabled, or data signal for 2-wire serial host interface. [Bi-directional, Schmitt trigger (400mV typical hysteresis), slew rate limited, 5V tolerant]
GPIO17 GPIO18 GPIO19 GPIO20	1 208 207 206	IO IO IO IO	General-purpose input/output signals. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]
GPIO21/IRQn	4	IO	General-purpose input/output signal when host port is disabled, or active-low and open-drain interrupt output pin. [Bi-directional, 5V-tolerant]
GPIO22/HCLK	204	IO	General-purpose input/output signal when host port is disabled, or clock for 2-wire serial host interface. [Bi-directional, Schmitt trigger (400mV typical hysteresis), 5V-tolerant]

Table 5. Display Output Port

Pin Name	No	I/O	Description
DCLK/TCON_OCLK	118	O	Panel output clock or TCON Odd Column Driver Bus Clock. [Tri-state output, Programmable Drive]
DVS/TCON_FSYNC	117	O	Panel Vertical Sync or TCON Frame Synchronization. [Tri-state output, Programmable Drive]
DHS/TCON_LP	116	O	Panel Horizontal Sync or TCON Load Pulse. [Tri-state output, Programmable Drive]
DEN/TCON_ECLK	115	O	Panel Display Enable, which frames the output background window, or TCON Even Column Driver Bus Clock. [Tri-state output, Programmable Drive]
PBIAS	114	O	Panel Bias Control (back light enable) [Tri-state output, Programmable Drive]
PPWR	113	O	Panel Power Control [Tri-state output, Programmable Drive]
PD47	110	O	Panel or TCON output data.
PD46	109	O	[Tri-state output, Programmable Drive]
PD45	108	O	
PD44	107	O	
PD43	106	O	
PD42	105	O	
PD41	104	O	
PD40	103	O	
PD39	102	O	
PD38	101	O	
PD37	100	O	
PD36	99	O	
PD35	96	O	
PD34	95	O	
PD33	94	O	
PD32	93	O	
PD31	92	O	
PD30	91	O	
PD29	90	O	
PD28	87	O	
PD27	86	O	
PD26	85	O	
PD25	84	O	
PD24	83	O	
PD23	80	O	
PD22	79	O	
PD21	78	O	
PD20	77	O	
PD19	76	O	
PD18	75	O	
PD17	74	O	
PD16	73	O	
PD15	72	O	
PD14	71	O	
PD13	70	O	
PD12	69	O	
PD11	66	O	
PD10	65	O	
PD9	64	O	
PD8	63	O	
PD7	62	O	
PD6	61	O	
PD5	60	O	
PD4	59	O	
PD3	58	O	
PD2	57	O	
PD1	56	O	
PD0	55	O	

Table 6. Parallel ROM Interface Port

Pin Name	No	I/O	Description
ROM_ADDR15	8	IO	ROM address output. These pins also serve as 5V-tolerant bootstrap inputs on power up.
ROM_ADDR14	9	IO	
ROM_ADDR13	10	IO	
ROM_ADDR12	11	IO	
ROM_ADDR11	12	IO	
ROM_ADDR10	13	IO	
ROM_ADDR9	14	IO	
ROM_ADDR8	15	IO	
ROM_ADDR7	16	IO	
ROM_ADDR6	17	IO	
ROM_ADDR5	18	IO	
ROM_ADDR4	19	IO	
ROM_ADDR3	22	IO	
ROM_ADDR2	23	IO	
ROM_ADDR1	24	IO	
ROM_ADDR0	25	IO	
ROM_DATA7	28	I	5V-tolerant external PROM data input
ROM_DATA6	29	I	
ROM_DATA5	30	I	
ROM_DATA4	31	I	
ROM_DATA3	32	I	
ROM_DATA2	33	I	
ROM_DATA1	34	I	
ROM_DATA0	35	I	
ROM_Oen	36	O	External PROM data Output Enable

Table 7. TCON Output Port

Pin Name	No	I/O	Description
TCON_OSP	119	O	Odd Starting Pulse
TCON_OPOL	120	O	Odd Polarity
TCON_OINV	121	O	Odd Data Transmission Inversion
TCON_ESP	122	O	Even Starting Pulse
TCON_EPOL	123	O	Even Polarity
TCON_EINV	124	O	Even Data Transmission Inversion
TCON_RSP2	125	O	Row Starting Pulse for 2-Voltage Row Driver
TCON_RSP3	126	O	Row Starting Pulse for 3-Voltage Row Driver
TCON_RCLK	127	O	Row Shift Clock
TCON_ROE	128	O	Row Output Enable

Table 8. Reserved Pins

Pin Name	No	I/O	Description
Reserved	131	I	Tie to GND.
Reserved	132	I	Tie to GND.
N/C	142	O	No connect
N/C	200	O	No connect

Note that VDD pins having "_2.5" in their names should be connected to 2.5V power supplies. All other VDD pins should be connected to 3.3V power supplies.

Table 9. Power Pins for ADC Sampling Clock DDS

Pin Name	No	I/O	Description
AVDD_SDDS	146	AP	Analog power for the Source DDS. Connect to 3.3V supply. Must be bypassed with a 0.1uF capacitor to AVSS_SDDS pin (as close to the pin as possible).
AVSS_SDDS	145	AG	Analog ground for the Source DDS. Must be directly connected to the analog system ground.
VDD_SDDS	144	P	Digital power for the Source DDS. Connect to 3.3V supply.
VSS_SDDS	143	G	Digital ground for the Source DDS.

Table 10. Power Pins for Display Clock DDS

Pin Name	No	I/O	Description
AVDD_DDDS	141	AP	Analog power for Destination DDS. Connect to 3.3V supply. Must be bypassed with a 0.1uF capacitor to AVSS_DDDS pin (as close to the pin as possible).
AVSS_DDDS	140	AG	Analog ground for Destination DDS. Must be directly connected to the analog system ground plane.
VDD_DDDS	139	P	Digital power for the Destination DDS. Connect to 3.3V supply.
VSS_DDDS	138	G	Digital ground for the Destination DDS.

Table 11. I/O Power and Ground Pins

Pin Name	No	I/O	Description
RVDD	2 20 37 53 67 81 97 111 129	P P P P P P P P P	Connect to 3.3V supply. Must be bypassed with a 0.1uF capacitor to RVSS (as close to the pin as possible).
RVSS	3 21 38 54 68 82 98 112 130	G G G G G G G G G	Connect to digital ground.

Table 12. Core Power and Ground Pins

Pin Name	No	I/O	Description
CVDD_2.5	26 88 134 203	P P P P	Connect to 2.5V supply. Must be bypassed with a 0.1uF capacitor to CVSS (as close to the pin as possible).
CVSS	27 89 133 135 202	G G G G G	Connect to digital ground.

Note, "AP" indicates a power supply that is analog in nature and does not have large switching currents. These should be isolated from other digital supplies that do have large switching currents.

4. FUNCTIONAL DESCRIPTION

A functional block diagram is illustrated below. Each of the functional units shown is described in the following sections.

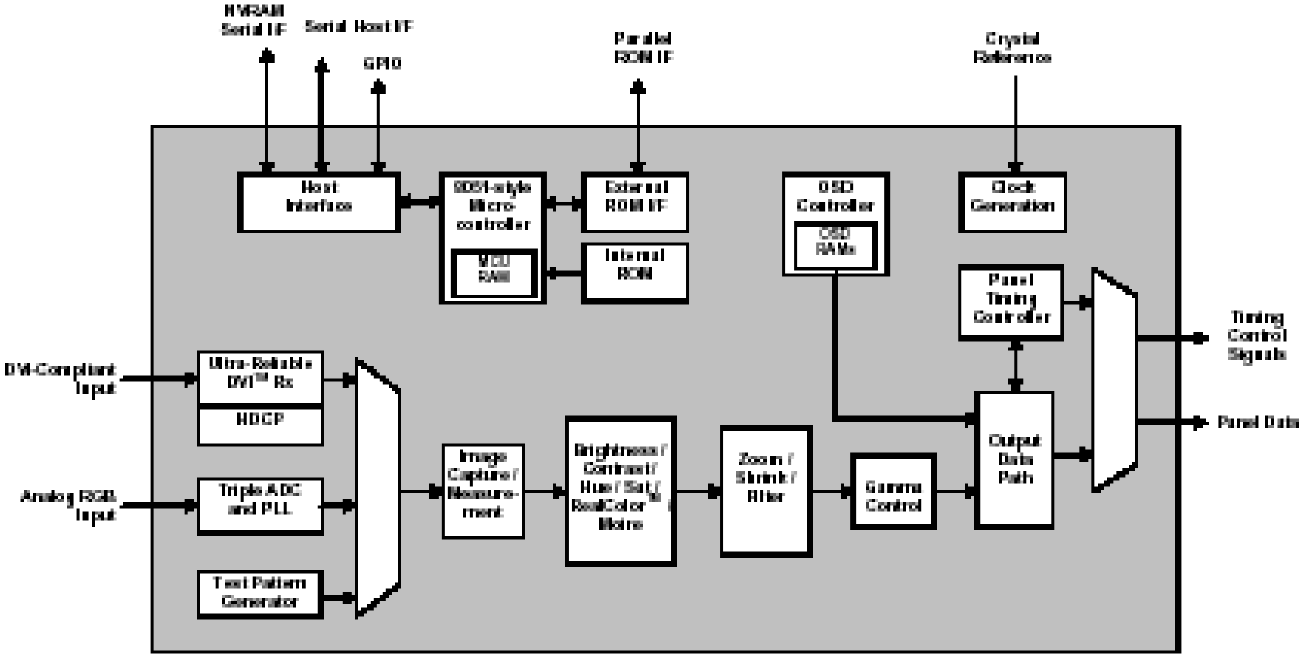


Figure 3. gm5115/25 Functional Block Diagram

4.1 Clock Generation

The gm5115/25 features three clock inputs. All additional clocks are internal clocks derived from one or more of these:

1. Crystal Input Clock (TCLK and XTAL). This is the input pair to an internal crystal oscillator and corresponding logic. A 14.3 MHz TV crystal is recommended. Other crystal frequencies may be used, but require custom programming. This is illustrated in Figure 4 below. Alternatively, a single-ended TTL/CMOS clock oscillator can be driven into the TCLK pin (leave XTAL as N/C in this case). This is illustrated in Figure 7 below. This option is selected by connecting a 10KΩ pull-up to ROM_ADDR13 (refer to Table 18). See also Table 14.
2. TMDS Differential Input Clock (RC+ and RC-)
3. Host Interface Transfer Clock (HCLK)

The gm5115 TCLK oscillator circuitry is a custom designed circuit to support the use of an external oscillator or a crystal resonator to generate a reference frequency source for the gm5115 device.

4.1.1 Using the Internal Oscillator with External Crystal

The first option for providing a clock reference is to use the internal oscillator with an external crystal. The oscillator circuit is designed to provide a very low jitter and very low harmonic clock to the internal circuitry of the gm5115. An Automatic Gain Control (AGC) is used to insure startup and operation over a wide range of conditions. The oscillator circuit also minimizes the overdrive of the crystal, which reduces the aging of the crystal.

When the gm5115/25 is in reset, the state of the ROM_ADDR13 pin (pin number 10) is sampled. If the pin is left unconnected (internal pull-down) then internal oscillator is enabled. In this mode a crystal resonator is connected between TCLK (pin 152) and the XTAL (pin 151) with the appropriately sized loading capacitors C_{L1} and C_{L2}. The size of C_{L1} and C_{L2} are determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the gm5115/25 device and the printed circuit board traces. The loading capacitors are terminated to the analog VDD power supply. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to ground.

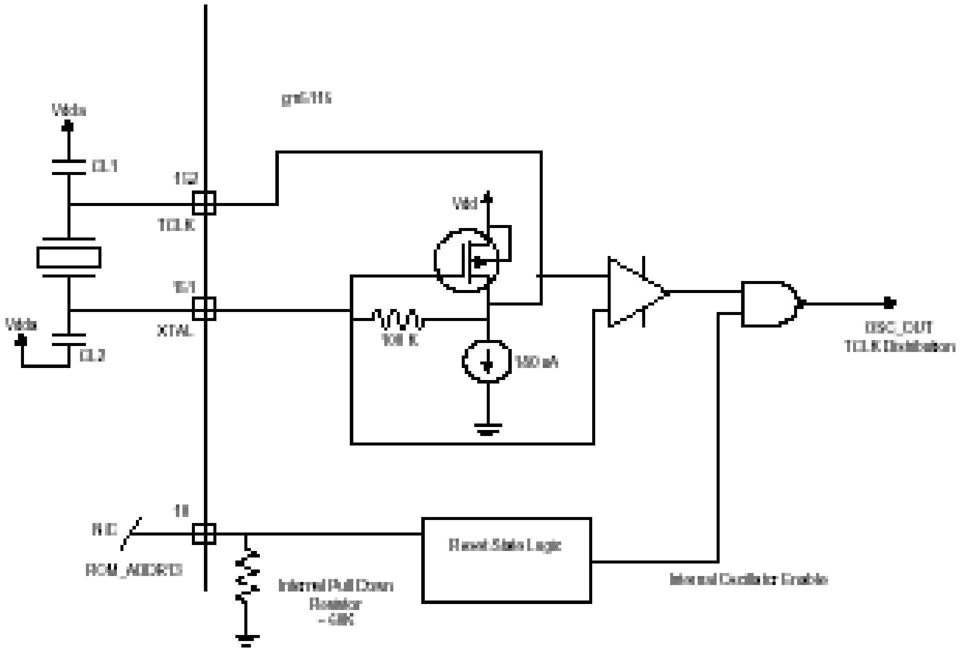


Figure 4. Using the Internal Oscillator with External Crystal

The TCLK oscillator uses a Pierce Oscillator circuit. The output of the oscillator circuit, measured at the TCLK pin, is an approximate sine wave with a bias of about 2 volts above ground (see Figure 5). The peak-to-peak voltage of the output can range from 250 mV to 1000 mV depending on the specific characteristics of the crystal and variation in the oscillator characteristics. The output of the oscillator is connected to a comparator that converts the sine wave to a square wave. The comparator requires a minimum signal level of about 50-mV peak to peak to function correctly. The output of the comparator is buffered and then distributed to the gm5115/25 circuits.

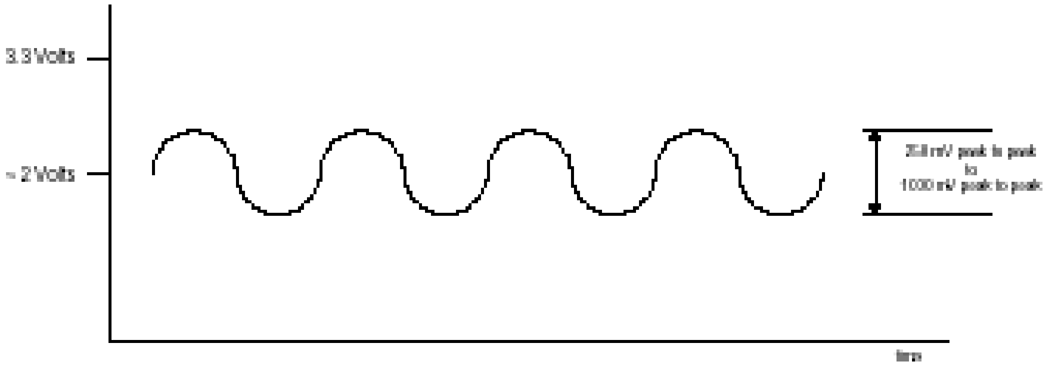


Figure 5. Internal Oscillator Output

One of the design parameters that must be given some consideration is the value of the loading capacitors used with the crystal as shown in Figure 6. The loading capacitance (C_{load}) on the crystal is the combination of C_{L1} and C_{L2} and is calculated by $C_{load} = ((C_{L1} * C_{L2}) / (C_{L1} + C_{L2})) + C_{shunt}$. The shunt capacitance C_{shunt} is the effective capacitance between the XTAL and TCLK pins. For the gm5115/25 this is approximately 9 pF. C_{L1} and C_{L2} are a parallel combination of the external loading capacitors (C_{ex}), the PCB board capacitance (C_{pcb}), the pin capacitance (C_{pin}), the pad capacitance (C_{pad}), and the ESD protection capacitance (C_{esd}). The capacitances are symmetrical so that $C_{L1} = C_{L2} = C_{ex} + C_{PCB} + C_{pin} + C_{pad} + C_{ESD}$. The correct value of C_{ex} must be calculated based on the values of the load capacitances. Approximate values are provided in Figure 6.

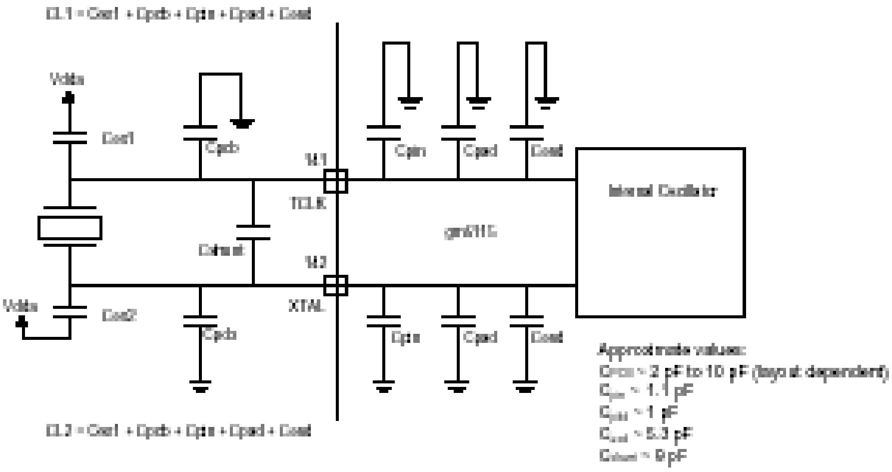


Figure 6. Sources of Parasitic Capacitance

Some attention must be given to the details of the oscillator circuit when used with a crystal resonator. The PCB traces should be as short as possible. The value of C_{load} that is specified by the manufacturer should not be exceeded because of potential start up problems with the oscillator. Additionally, the crystal should be a parallel resonate-cut and the value of the equivalent series resistance must be less then 90 Ohms.

4.1.2 Using an External Clock Oscillator

Another option for providing the reference clock is to use a single-ended external clock oscillator. When the gm5115/25 is in reset, the state of the ROM_ADDR13 (pin 10) is sampled. If ROM_ADDR13 is pulled high by connecting to VDD through a pull-up resistor (15KΩ recommended, 15KΩ maximum) then external oscillator mode is enabled. In this mode the internal oscillator circuit is disabled and the external oscillator signal that is connected to the TCLK pin (pin number 152) is routed to an internal clock buffer. This is illustrated in Figure 7.

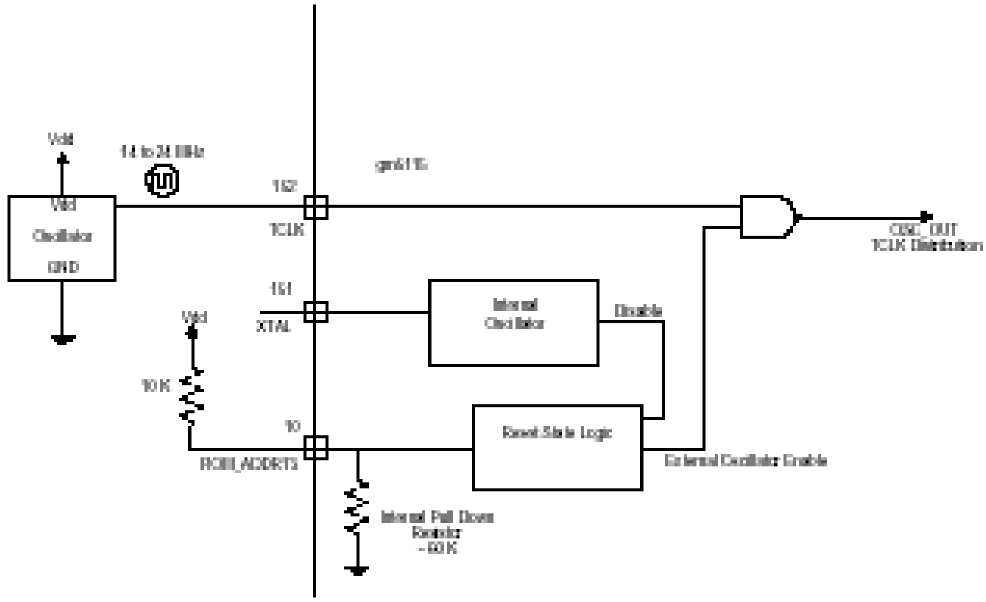


Figure 7. Using an External Single-ended Clock Oscillator

Frequency	14 to 24 MHz
Jitter Tolerance	250 ps
Rise Time (10% to 90%)	5 ns
Maximum Duty Cycle	40-60

Table 13. TCLK Specification

4.1.3 Clock Synthesis

The gm5115/25 synthesis all additional clocks internally as illustrated in Figure 8 below. The synthesized clocks are as follows:

1. Main Timing Clock (TCLK) is the output of the chip internal crystal oscillator. TCLK is derived from the TCLK/XTAL pad input.
2. Reference Clock (RCLK) synthesized by RCLK PLL (RPLL) using TCLK as the reference.
3. TMDS Input Clock (TMDS_CLK) synthesized by TMDS receiver PLL using RC+/RC- pair as the reference.
4. Input Source Clock (SCLK) synthesized by Source DDS (SDDS) PLL using input HSYNC as the reference. The SDDS internal digital logic is driven by RCLK.

5. Display Clock (DCLK) synthesized by Destination DDS (DDDS) PLL using IP_CLK as the reference. The DDDS internal digital logic is driven by RCLK.
6. Half Reference Clock (RCLK/2) is the RCLK (see 2, above) divided by 2. Used as OCM_CLK domain driver.
7. Quarter Reference Clock (RCLK/4) is the RCLK (see 2, above) divided by 4. Used as alternative clock (faster than TCLK) to drive IFM.
8. ADC Output Clock (SENSE_ACLK) is a delay-adjusted ADC sampling clock, ACLK. ACLK is derived from SCLK.

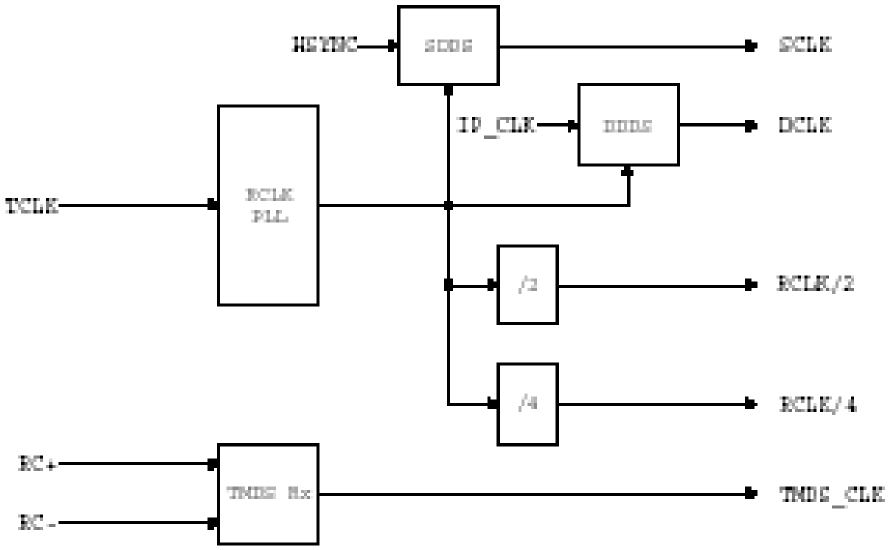


Figure 8. Internally Synthesized Clocks

The on-chip clock domains are selected from the synthesized clocks as shown in Figure 9 below. These include:

1. Input Domain Clock (IP_CLK). Max = 165MHz
2. Host Interface and On-Chip Microcontroller Clock (OCM_CLK). Max = 100MHz
3. Filter and Display Pixel Clock (DP_CLK). Max = 135MHz
4. Source Timing Measurement Domain Clock (IFM_CLK). Max = 50MHz
5. ADC Domain Clock (ACLK). Max = 165MHz.

The clock selection for each domain as shown in the figure below is controlled using the CLOCK_CONFIG registers (index 0x03 and 0x04).

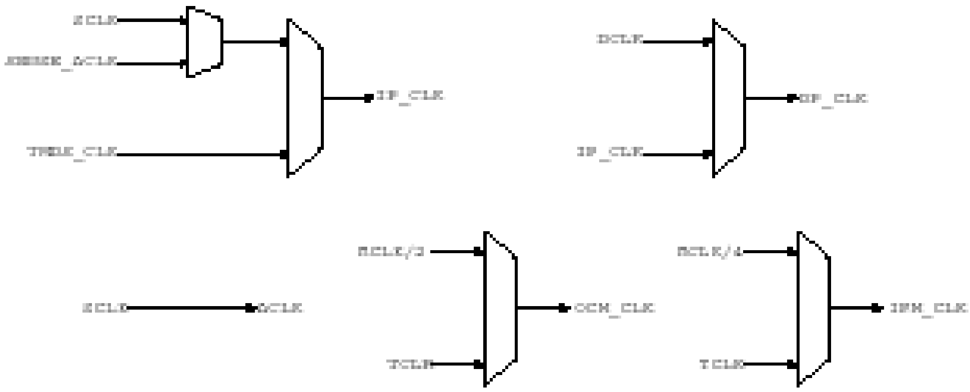


Figure 9. On-chip Clock Domains

4.2 Hardware Reset

Hardware Reset is performed by holding the RESETn pin low for a minimum of 1µs. A TCLK input (see Clock Options above) must be applied during and after the reset. When the reset period is complete and RESETn is de-asserted, the power-up sequence is as follows:

1. Reset all registers of all types to their default state (this is 00h unless otherwise specified in the gm5115/25 Register Listing).
2. Force each clock domain into reset. Reset will remain asserted for 64 local clock domain cycles following the de-assertion of RESETn.
3. Operate the OCM_CLK domain at the TCLK frequency.
4. Preset the RCLK PLL to output ~200MHz clock (assumes 14.3MHz TCLK crystal frequency).
5. Wait for RCLK PLL to Lock. Then, switch the OCM_CLK domain to operate from the bootstrap selected clock.
6. If a pull-up resistor is installed on ROM_ADDR9 pin (see Table 18), then the OCM becomes active as soon as OCM_CLK is stable. Otherwise, the OCM remains in reset until OCM_CONTROL register (0x22) bit 1 is enabled.

4.3 Analog to Digital Converter (ADC)

The gm5115/25 chip has three ADC's (analog-to-digital converters), one for each color (red, green, and blue).

4.3.1 ADC Pin Connection

The analog RGB signals are connected to the gm5115/25 as described below:

Table 14. Pin Connection for RGB Input with HSYNC/VSYNC

Pin Name	ADC Signal Name
Red+	Red
Red-	Terminate as illustrated in Figure 10
Green+	Green
Green-	Terminate as illustrated in Figure 10
Blue+	Blue
Blue-	Terminate as illustrated in Figure 10
HSYNC	Horizontal Sync (Terminate as illustrated in Figure 10)
VSYNC	Vertical Sync (Terminate as with HSYNC illustrated in Figure 10)

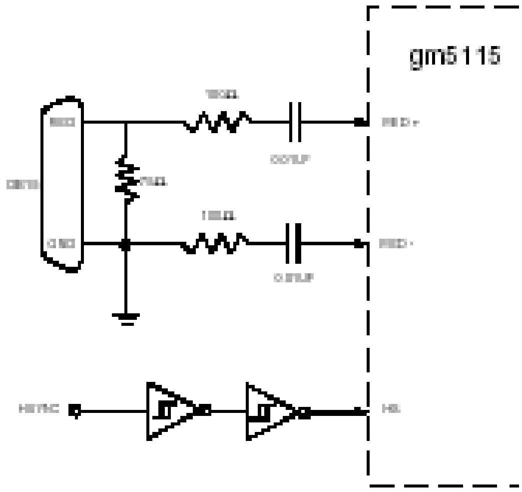


Figure 10. Example ADC Signal Terminations

Please note that it is very important to follow the recommended layout guidelines for the circuit shown in Figure 10. These are described in "gm5115/25 Layout Guidelines" document number C5115-SLG-01A.

4.3.2 ADC Characteristics

The table below summarizes the characteristics of the ADC:

Table 15. ADC Characteristics

	MIN	TYP	MAX	NOTE
Track & Hold Amp Bandwidth		290 MHz		Guaranteed by design. Note that the Track & Hold Amp Bandwidth is programmable. 290 MHz is the maximum setting.
Full Scale Adjust Range at RGB Inputs	0.55 V		0.90 V	
Full Scale Adjust Sensitivity		+/- 1 LSB		Measured at ADC Output. Independent of full-scale RGB input
Zero Scale Adjust Sensitivity		+/- 1 LSB		Measured at ADC Output.
Sampling Frequency (Fs)	10 MHz		162.5 MHz	
Differential Non-Linearity (DNL)		+/-0.5 LSB	+/-0.9 LSB	Fs = 135 MHz
No Missing Codes				Guaranteed by test
Integral Non-Linearity (INL)		+/- 1.5LSB		Fs =135 MHz
Channel to Channel Matching		+/- 0.5LSB		

The gm5115/25 ADC has a built-in clamp circuit for AC-coupled inputs. By inserting series capacitors (about 10 nF), the DC offset of an external video source can be removed. The clamp pulse position and width are programmable.

4.3.3 Clock Recovery Circuit

The SDDS (Source Direct Digital Synthesis) clock recovery circuit generates the clock used to sample analog RGB data (IP_CLK or source clock). This circuit is locked to HSYNC of the incoming video signal.

Patented digital clock synthesis technology makes the gm5115/25 clock circuits resistant to temperature/voltage drift. Using DDS (Direct Digital Synthesis) technology, the clock recovery circuit can generate any IP_CLK clock frequency within the range of 10MHz to 165MHz.

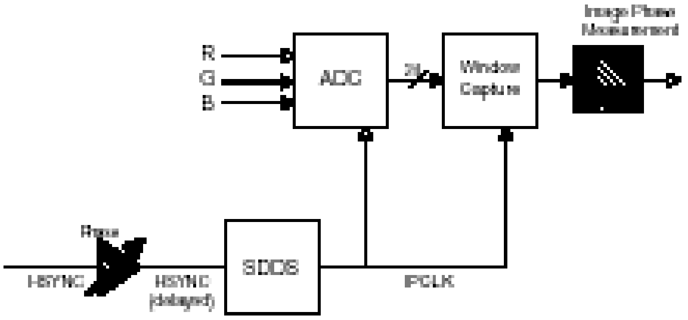


Figure 11. gm5115/25 Clock Recovery

4.3.4 Sampling Phase Adjustment

The programmable ADC sampling phase is adjusted by delaying the HSYNC input to the SDDS. The accuracy of the sampling phase is checked and the result read from a register. This feature enables accurate auto-adjustment of the ADC sampling phase.

4.3.5 ADC Capture Window

Figure 12 below illustrates the capture window used for the ADC input. In the horizontal direction the capture window is defined in IP_CLKs (equivalent to a pixel count). In the vertical direction it is defined in lines.

All the parameters beginning with "Source" are programmed gm5115/25 registers values. Note that the Input Vertical Total is solely determined by the input and is not a programmable parameter.

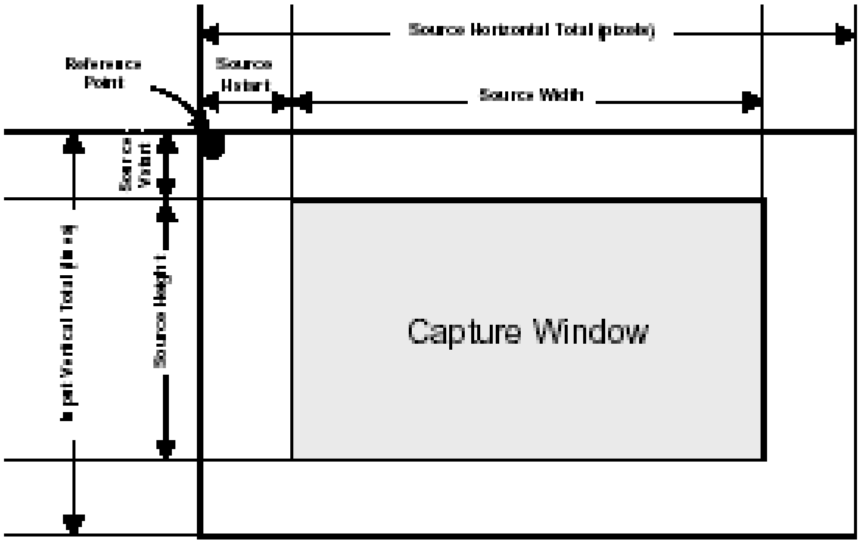


Figure 12. ADC Capture Window

The Reference Point marks the leading edge of the first internal HSYNC following the leading edge of an internal VSYNC. Both the internal HSYNC and the internal VSYNC are derived from external HSYNC and VSYNC inputs.

Horizontal parameters are defined in terms of single pixel increments relative to the internal horizontal sync. Vertical parameters are defined in terms of single line increments relative to the internal vertical sync.

For ADC interlaced inputs, the gm5115/25 may be programmed to automatically determine the field type (even or odd) from the VSYNC/HSYNC relative timing. See Input Format Measurement, Section 4.6.

4.4 Ultra-Reliable Digital Visual Receiver (DVI Rx)

The Ultra-Reliable DVI™ receiver block of the gm5115/25 is compliant with DVI1.0 single link specifications. Digital Visual Interface (DVI) is a standard that uses Transition Minimized Differential Signaling protocol (TMDS). This block supports an input clock frequency ranging from 20 MHz to 165 MHz.

4.4.1 DVI Receiver Characteristics

Table 16 summarizes the characteristics of the four Receiver Pair inputs. Please note that it is very important to follow the recommended layout guidelines for these signals. These are described in "gm5115/25 Layout Guidelines" document number C5115-SLG-01A.

Table 16. DVI Receiver Characteristics

	MIN	TYP	MAX	NOTE
DC Characteristics				
Differential Input Voltage	150mV		1200mV	
Input Common Mode Voltage	AVDD –300mV		AVDD -37mV	
Behavior when Transmitter Disable	AVDD -10mV		AVDD +10mV	
AC Characteristics				
Input clock frequency	20 MHz		165 MHz	
Input differential sensitivity (Peak-to-peak)	150mV			
Max differential input (peak-to-peak)			1560 mV	
Allowable Intra-Pair skew at Receiver			250 ps	Input clock = 160 MHz
Allowable Inter-Pair skew at Receiver			4.0 ns	
Worst case differential input clock jitter tolerance			188 ps	

Through register programming, the receiver unit may be placed in one of three states:

- **Active:** The receiver block is fully on and running.
- **Standby:** Only the RC (clock) channel remains active. Data and other control signals are not decoded.
- **Off:** The receiver block is powered down.

4.4.2 DVI Capture Window

DE (Display Enable), HSYNC and VSYNC are synthesized internally by examining the active regions of each line and compensating for possible source timing errors and/or embedded HSYNC / VSYNC jitter.

There are two ways to define the DVI capture region:

CREF Capture - In this mode the usual active window parameters must be programmed as with ADC inputs (see Section 4.3.5.).

DE Capture - In this mode the active window code embedded in the TMDS signal defines the active window automatically. Only the active width and active length parameters obtained by performing Input Format Measurement (IFM) need be programmed.

4.4.3 High-Bandwidth Digital Content Protection (HDCP)

The HDCP system allows authentication of a video receiver by a video transmitter, decryption of transmitter-encoded video data by the receiver, and periodic renew-ability of authentication during transmission. The gm5115/25 implements circuitry to allow full support of the HDCP 1.0 protocol for DVI inputs.

For enhanced security, Genesis provides a means of storing and accessing the secret key given to individual monitor units in an encrypted format.

Further details of the protocol and theory of the system can be found in the *High-bandwidth Digital Content Protection System* specification (see www.digital-cp.com).

4.5 Test Pattern Generator (TPG)

The gm5115/25 contains hundreds of test patterns, some of which are shown in Figure 13. Once programmed, the gm5115/25 test pattern generator can replace a video source (e.g. a PC) during factory calibration and test. This simplifies the test procedure and eliminates the possibility of image noise being injected into the system from the source. The foreground and background colors are programmable. In addition, the gm5115/25 OSD controller can be used to produce other patterns.

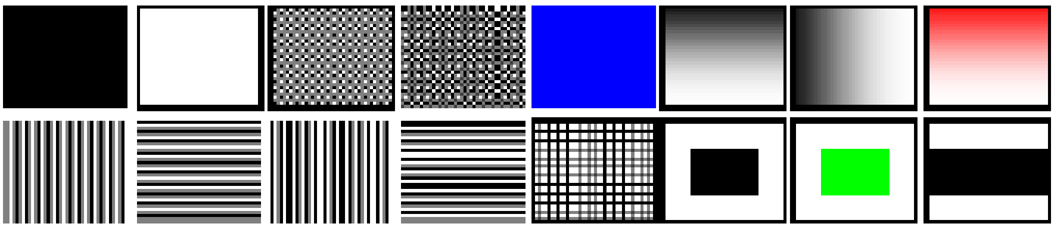


Figure 13. Some of gm5115/25 built-in test patterns

4.6 Input Format Measurement (IFM)

The gm5115/25 has an Input Format Measurement block (the IFM) providing the capability of measuring the horizontal and vertical timing parameters of the input video source. This information may be used to determine the video format and to detect a change in the input format. It is also capable of detecting the field type of interlaced formats.

The IFM features a programmable reset, separate from the regular gm5115/25 soft reset. This reset disables the IFM, reducing power consumption. The IFM is capable of operating while the gm5115/25 is running in power-down mode.

Horizontal measurements are measured in terms of the selected IFM_CLK (either TCLK or RCLK/4), while vertical measurements are measured in terms of HSYNC pulses.

For an overview of the internally synthesized clocks, see section 4.1.

4.6.1 HSYNC / VSYNC Delay

The active input region captured by the gm5115/25 is specified with respect to internal HSYNC and VSYNC. By default, internal syncs are equivalent to the HSYNC and VSYNC at the input pins and thus force the captured region to be bounded by external HSYNC and VSYNC timing. However, the gm5115/25 provides an internal HSYNC and VSYNC delay feature that removes this limitation. This feature is available for use with both the ADC input and the DVI Rx (DE-regeneration mode). By delaying the sync internally, the gm5115/25 can capture data that spans across the sync pulse.

It is possible to use HSNYC and VSYNC delay for image positioning. (Alternatively, Source_HSTART and Source_VSTART in Figure 12 are used for image positioning of analog input.) Taken to an extreme, the intentional movement of images across apparent HSYNC and VSYNC boundaries creates a horizontal and/or vertical wrap effect.

HSYNC is delayed by a programmed number of selected input clocks.

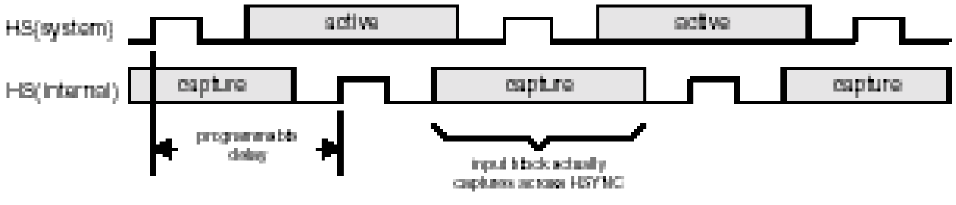


Figure 14. HSYNC Delay

Delayed horizontal sync may be used to solve a potential problem with VSYNC jitter with respect to HSYNC. VSYNC and HSYNC are generally driven active coincidentally, but with different paths to the gm5115/25 (HSYNC is often regenerated from a PLL). As a result, VSYNC may be seen earlier or later. Because VSYNC is used to reset the line

counter and HSYNC is used to increment it, any difference in the relative position of HSYNC and VSYNC is seen on-screen as vertical jitter. By delaying the HSYNC a small amount, it can be ensured that VSYNC always resets the line counter prior to it being incremented by the "first" HSYNC.

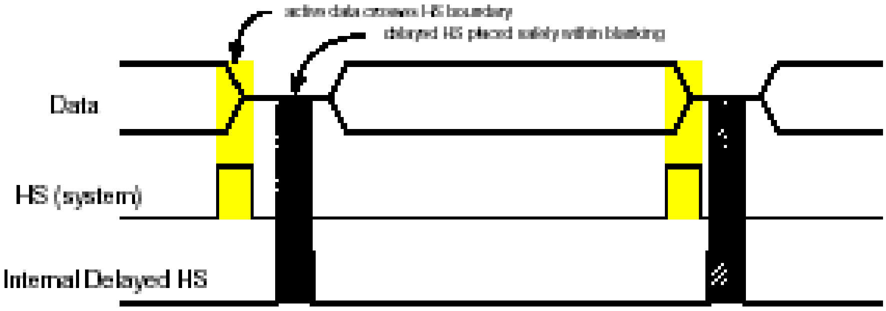


Figure 15. Active Data Crosses HSYNC Boundary

4.6.2 Horizontal and Vertical Measurement

The IFM is able to measure the horizontal period and active high pulse width of the HSYNC signal, in terms of the selected clock period (either TCLK or RCLK/4.). Horizontal measurements are performed on only a single line per frame (or field). The line used is programmable. It is able to measure the vertical period and VSYNC pulse width in terms of rising edges of HSYNC.

Once enabled, measurement begins on the rising VSYNC and is completed on the following rising VSYNC. Measurements are made on every field / frame until disabled.

4.6.3 Format Change Detection

The IFM is able to detect changes in the input format relative to the last measurement and then alert both the system and the on-chip microcontroller. The microcontroller sets a measurement difference threshold separately for horizontal and vertical timing. If the current field / frame timing is different from the previously captured measurement by an amount exceeding this threshold, a status bit is set. An interrupt can also be programmed to occur.

4.6.4 Watchdog

The watchdog monitors input VSYNC / HSYNC. When any HSYNC period exceeds the programmed timing threshold (in terms of the selected IFM_CLK), a register bit is set. When any VSYNC period exceeds the programmed timing threshold (in terms of HSYNC pulses), a second register bit is set. An interrupt can also be programmed to occur.

4.6.5 Internal Odd/Even Field Detection

The IFM has the ability to perform field decoding of interlaced inputs to the ADC. The user specifies start and end values to outline a "window" relative to HSYNC. If the VSYNC leading edge occurs within this window, the IFM signals the start of an ODD field. If the VSYNC leading edge occurs outside this window, an EVEN field is indicated (the interpretation of odd and even can be reversed). The window start and end points are selected from a predefined set of values.

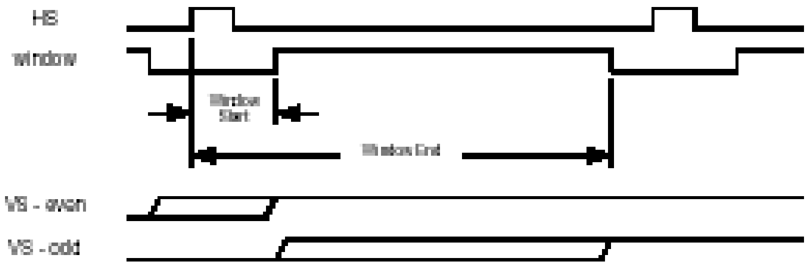


Figure 16. ODD/EVEN Field Detection

4.6.6 Input Pixel Measurement

The gm5115/25 provides a number of pixel measurement functions intended to assist in configuring system parameters such as pixel clock, SDDS sample clocks per line and phase setting, centering the image, or adjusting the contrast and brightness.

4.6.7 Image Phase Measurement

This function measures the sampling phase quality over a selected active window region. This feature may be used when programming the source DDS to select the proper phase setting. Please refer to the gm5115/25 Programming Guide for the optimized algorithm.

4.6.8 Image Boundary Detection

The gm5115/25 performs measurements to determine the image boundary. This information is used when programming the Active Window and centering the image.

4.6.9 Image Auto Balance

The gm5115/25 performs measurements on the input data that are used to adjust brightness and contrast.

4.7 RealColor™ Digital Color Controls

The gm5115/25 provides high-quality digital color controls. These consist of a subtractive "black level" stage, followed by a full 3x3 RGB matrix multiplication stage, followed by an signed offset stage as shown in Figure 17.

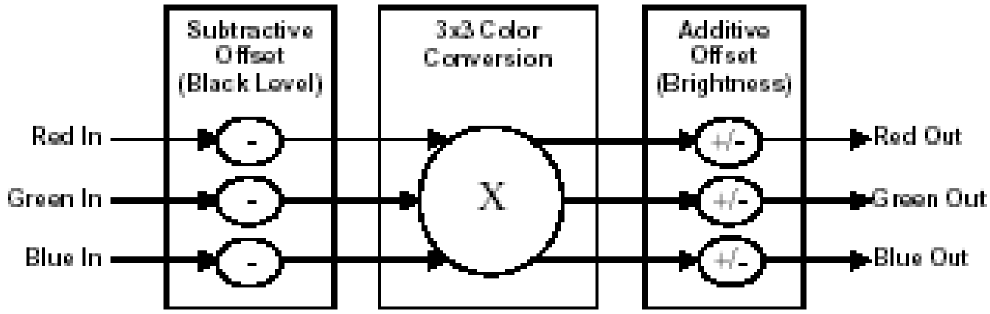


Figure 17. RealColor™ Digital Color Controls

This structure can accommodate all RGB color controls such as black-level (subtractive stage), contrast (multiplicative stage), and brightness (signed additive offset). In addition, it supports all YUV color controls including brightness (additive factor applied to Y), contrast (multiplicative factor applied to Y), hue (rotation of U and V through an angle) and saturation (multiplicative factor applied to both Y and V).

To provide the highest color purity all mathematical functions use 10 bits of accuracy. The final result is then dithered to eight or six bits (as required by the LCD panel).

4.7.1 RealColor™ Flesh tone Adjustment

The human eye is more sensitive to variations of flesh tones than other colors; for example, the user may not care if the color of grass is modified slightly during image capture and/or display. However, if skin tones are modified by even a small amount, it is unacceptable. The gm5115/25 features flesh tone adjustment capabilities. This feature is not based on lookup tables, but rather a manipulation of YUV-channel parameters. Flesh tone adjustment is available for all inputs.

4.7.2 Color Standardization and sRGB Support

Internet shoppers may be very picky about what color they experience on the display. gm5115/25 RealColor™ digital color controls can be used to make the color response of an LCD monitor compliant with standard color definitions, such as sRGB. sRGB is a standard for color exchange proposed by Microsoft and HP (see www.srgb.com). gm5115/25 RealColor controls can be used to make LCD monitors sRGB compliant, even if the native

response of the LCD panel itself is not. For more information on sRGB compliance using gm5115/25 family devices please refer to the sRGB application brief C5115-APB-02A.

4.8 High-Quality Scaling

The gm5115/25 zoom/shrink scaler uses an adaptive scaling technique proprietary to Genesis Microchip Inc., and provides high quality scaling of real time video and graphics images. An input field/frame is scalable in both the vertical and horizontal dimensions.

Interlaced fields may be spatially de-interlaced by vertically scaling and repositioning the input fields to align with the output display's pixel map.

4.8.1 Variable Zoom Scaling

The gm5115/25 scaling filter can combine its advanced scaling with a pixel-replication type scaling function. This is useful for improving the sharpness and definition of graphics when scaling at high zoom factors (such as VGA to XGA).

4.8.2 Horizontal and Vertical Shrink

A shrink function may be performed on the input data. This is an arbitrary horizontal active resolution reduction to between (50% + 1 pixel) to 100% of the input. For example, this allows SXGA 1280 pixels to be displayed as 1024 (XGA).

The gm5115/25 provides an arbitrary vertical shrink down to (50% + 1 line) of the original image size. Together with the arbitrary horizontal shrink, this allows the gm5115/25 to capture and display images one VESA standard format larger than the native display resolution. For example, SXGA may be captured and displayed on an XGA panel.

4.8.3 Moiré Cancellation

The gamma curve and other non-linearities can affect the energy distribution of pixels when scaled to different areas of the screen. This is an example of the Moiré effect. The gm5115/25 has hardware features to negate the Moiré effect, improving the scaling quality.

4.9 Bypass Options

The gm5115/25 has the capability to completely bypass internal processing. In this case, captured input signals and data are passed, with a small latency, straight through to the display output. The gm5115/25 is also able to bypass the zoom filter and the gamma LUT.

4.10 Gamma Look-Up-Table (LUT)

The gm5115/25 provides an 8 to 10-bit look-up table (LUT) for each input color channel intended for Gamma correction and to compensate for a non-linear response of the LCD panel. A 10-bit output results in an improved color depth control. The 10-bit output is then dithered down to 8 bits (or 6 bits) per channel at the display (see section 4.11.3 below). The LUT is user-programmable to provide an arbitrary transfer function. Gamma correction occurs after the zoom / shrink scaling block. If bypassed, the LUT does not require programming.

4.11 Display Output Interface

The Display Output Port provides data and control signals that permit the gm5115/25 to connect to a variety of flat panel or CRT devices. The output interface is configurable for 18 or 24-bit RGB pixels, either single- or double-pixel wide. All display data and timing signals are synchronous with the DCLK output clock.

4.11.1 Display Synchronization

Refer to section 4.1 for information regarding internal clock synthesis.

The gm5115/25 supports the following display synchronization modes:

- **Frame Sync Mode:** The display frame rate is synchronized to the input frame or field rate. This mode is used for standard operation.
- **Free Run Mode:** No synchronization. This mode is used when there is no valid input timing (i.e. to display OSD messages or a splash screen) or for testing purposes. In free-run mode, the display timing is determined only by the values programmed into the display window and timing registers.

4.11.2 Programming the Display Timing

Display timing signals provide timing information so the Display Port can be connected to an external display device. Based on values programmed in registers, the Display Output Port produces the horizontal sync (DHS), vertical sync (DVS), and data enable (DEN) control signals. The figure below provides the registers that define the output display timing.

Horizontal values are programmed in single-pixel increments relative to the leading edge of the horizontal sync signal. Vertical values are programmed in line increments relative to the leading edge of the vertical sync signal.

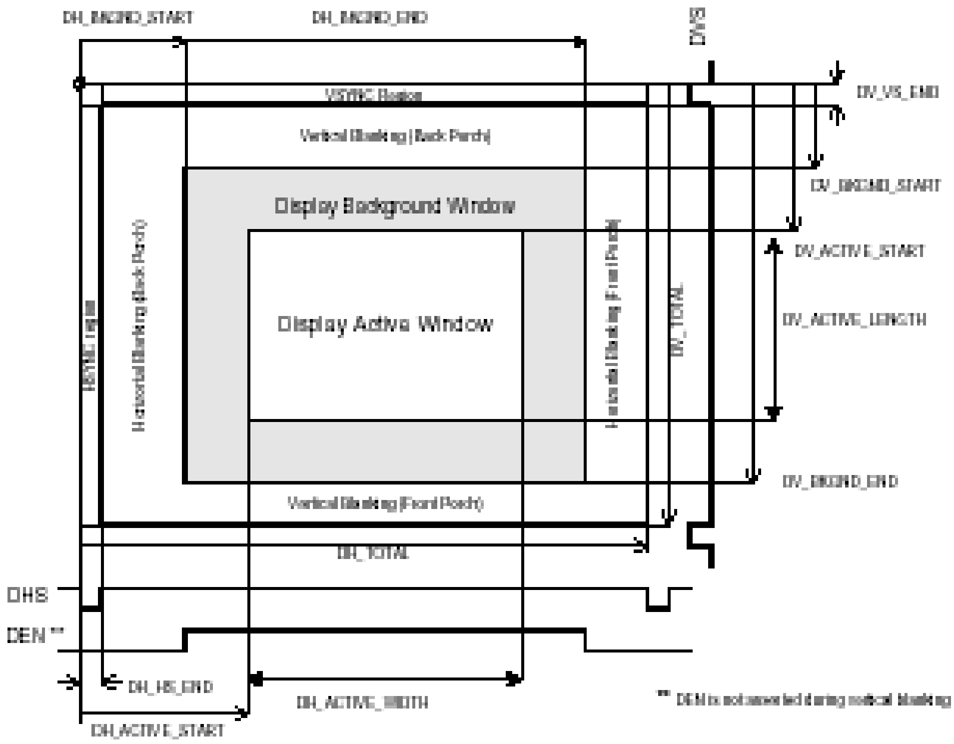


Figure 18. Display Windows and Timing

The double-wide output only supports an even number of horizontal pixels.

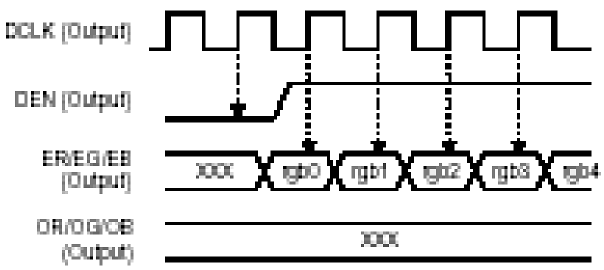


Figure 19. Single Pixel Width Display Data

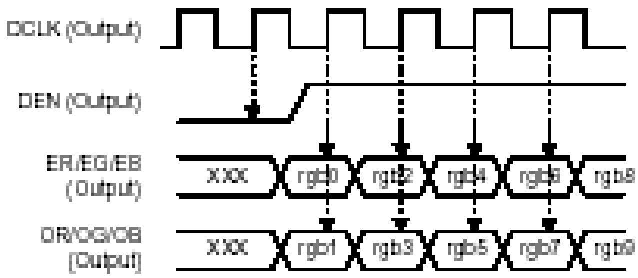


Figure 20. Double Pixel Wide Display Data

4.11.3 Panel Power Sequencing (PPWR, PBIAS)

The gm5115/25 has two dedicated outputs PPWR and PBIAS (pins 113 and 114) to control LCD power sequencing once data and control signals are stable. The timing of these signals is fully programmable.

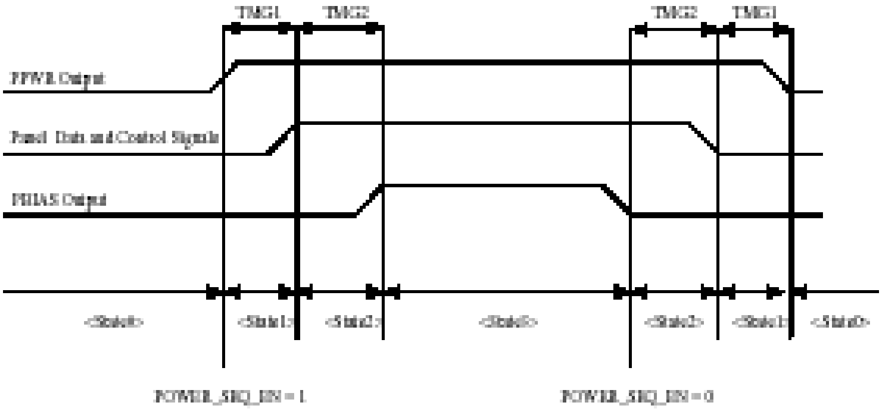


Figure 21. Panel Power Sequencing

4.11.4 Output Dithering

The Gamma LUT outputs a 10-bit value for each color channel. This value is dithered down to either 8-bits for 24-bit per pixel panels, or 6-bits for 18-bit per pixel panels.

The benefit of dithering is that the eye tends to average neighboring pixels and a smooth image free of contours is perceived. Dithering works by spreading the quantization error over neighboring pixels both spatially and temporally. Two dithering algorithms are available: random or ordered dithering. Ordered dithering is recommended when driving a 6-bit panel.

All gray scales are available on the panel output whether using 8-bit panel (dithering from 10 to 8 bits per pixel) or using 6-bit panel (dithering from 10 down to 6 bits per pixel).

4.12 Timing Controller (TCON)

The gm5115/25 features an integrated timing controller (TCON) that connects directly to commercially available row and column drivers. It supports either 18 or 24-bits per pixel in 1 or 2 pixels per clock XGA operation. Also, it supports single or dual-edge clocking modes. Frame, Line (Row) and pixel inversion is available for better image quality. In-Line inversion reduces power consumption and EMI radiation. Data signals have programmable drive strength.

During panel power-up the TCON control signals can be held inactive. This is to provide correct power sequencing that does not damage the panel. The TCON control signals only become active when the panel power sequencing is complete.

4.12.1 Programmable Column Driver Interface

The gm5115/25 column driver interface is highly programmable. It supports dual bus / dual port, dual bus / one port (both interleave and bank) as well as single bus / single port for XGA column drivers.

The column driver interface consists of the following signals:

OCLK/ECLK – Odd/Even Column Driver bus clock. OCLK and ECLK have a programmable phase control (0-7ns) and programmable polarities. Even output data bus (ERGB) can be skewed ½ clock (early) to reduce the number of outputs switching simultaneously.

OSP/ESP - Odd/Even Starting Pulse. OSP and ESP have programmable positioning before valid data. They also have programmable polarities.

ORGB[24]/ERGB[24] – Odd/Even 24 bits data bus supports 24 or 18 bits per pixel in 1 or 2 pixels per clock. These signals support even/odd, red/blue and data bit swap. They also have programmable group and inter-group delays (0-7ns).

OPOL/EPOL – Odd/Even polarity. With programmable position of OPOL/EPOL, the OPOL/EPOL can be switched when LP is active or before or after LP.

OINV/EINV – Odd/Even data transition inversion. These signals provide data inversion capability to reduce electromagnetic interference (EMI). One INV signal can be used (either EINV or OINV), or both.

LP – Load/Latch pulse. The Load/Latch pulse has a programmable width and polarity.

SHC – Output circuit control. This signal has programmable timing similar to OPOL/EPOL. It is optionally available on GPIO6.

TDIV – Horizontal timing. This signal rises with LP and has a programmable falling edge. It is optionally available on GPIO7.

All signals OCLK, ECLK, ORGB, ERGB, OSP, ESP, OPOL, EPOL, OINV, EINV have programmable drive strengths and can be disabled.

Clocks (OCLK/ECLK), Polarities (EPOL/OPOL) and Data (ERGB/ORGB, ESP/OSP) can be blanked separately, during horizontal and/or vertical blanking period (programmable) to reduce power. Clocks and Polarities are forced to zero and Data (ERGB/ORGB) is forced to either white or black during blanking period.

Refer to Figure 22 for the column driver interface timing. See the gm5115/25 programming guide (C5115-DSR-01) for details regarding column driver programming.

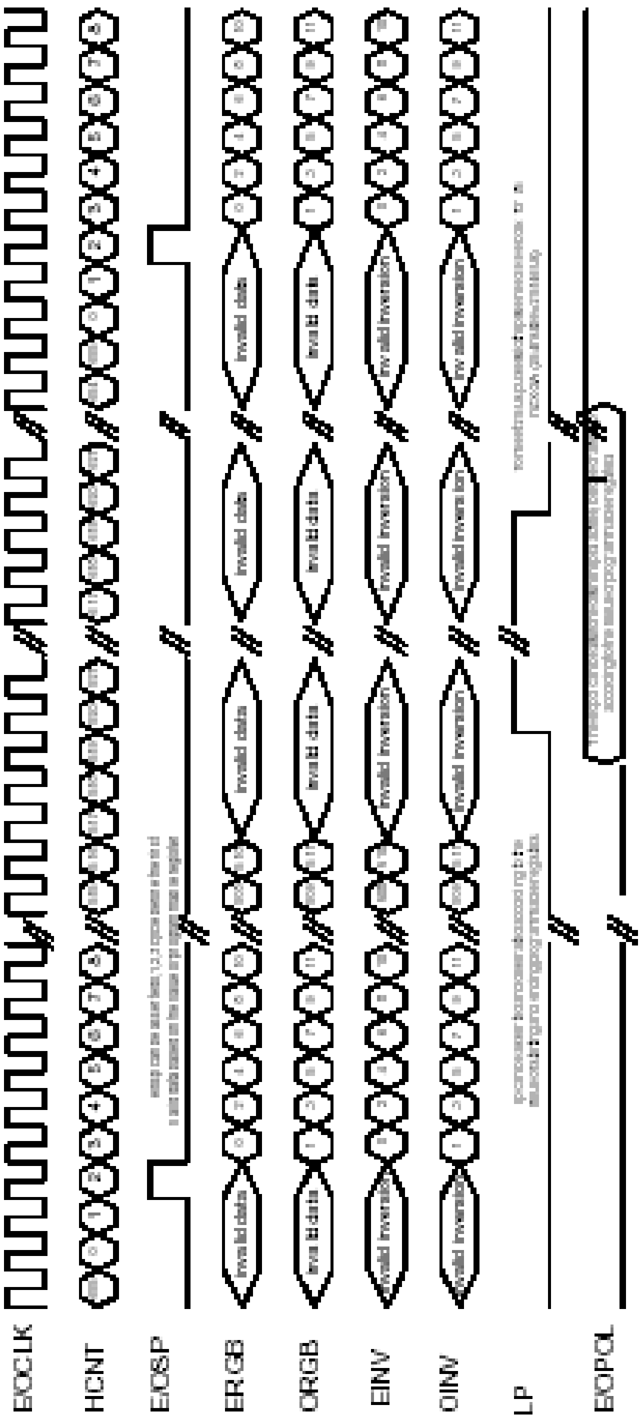


Figure 22. Column Driver Interface Timing

4.12.2 Programmable Row Driver Interface

The gm5115/25 row driver interface supports 2 and 3 voltage row drivers.

The row driver interface consists of the following signals. The starting time and pulse-width of each are fully programmable.

RSP2 – Row Starting Pulse for 2 voltage Row Driver

RSP3 – Row Starting Pulse for 3 voltage Row Driver

RCLK – Row/Vertical shift clock

ROE – Row Output Enable or Row Blank Time or Gate Driver Output Enable. This signal is used to control RC discharge time. Note that some vendors support three ROE's for this function to avoid 2 lines being activated at the same time (ROE2 and ROE3 are optionally available on pins GPIO9 and GPIO10). The polarities of ROE, ROE2 and ROE3 are programmable. These signals can be blanked during horizontal and/or vertical blanking to reduce power. In addition, ROE, ROE2 and ROE3 may be staggered.

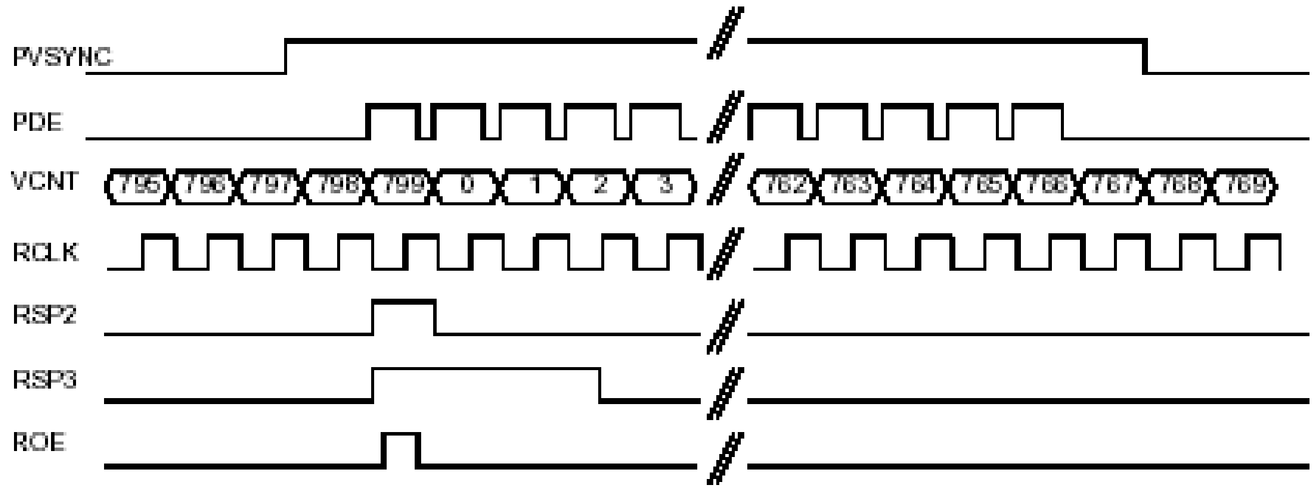
RCLK, ROE, ROE2 and ROE3 have programmable polarities and can be blanked during horizontal and/or vertical blanking period (programmable) to reduce power. Note that ROE2 and ROE3 can be used to drive GV and GVOFF signals required by some row driver ICs.

See the gm5115/25 programming guide (C5115-DSR-01) for details regarding row driver programming.

4.12.3 Reduced EMI

The gm5115/25 programmable TCON has many features that can be used to reduce electromagnetic interference (EMI). These include transition minimization, data staggering, data swapping for reduced trace length (even with odd, red with blue and bit 0 with bit 7), slew rate control and dual-edge clocking.

In addition, the DP_CLK generation circuit features a proprietary method for the reduction of electromagnetic interference (EMI) emitted by the display port. High spikes in the EMI power spectrum may cause LCD monitor products to violate emissions standards.



Notes:
1. The rclk low and high time can be determined by horizontal starting and ending programmable registers
2. The pulse width of RSP2 and RSP3 based on number of rclks can be determined by vertical starting and ending programmable registers
3. The pulse width of ROE can be determinded by horizontal starting and ending programmable registers
4. For example, For 75 Hz XGA the Hor Total Time is 1312x12.7ns = 16.6 us, the low/high time of rclk is 16.6 us/2 = 328 ecoclk

Figure 23. Row Driver Interface Timing

4.13 OSD

The gm5115/25 has a fully programmable, high-quality OSD controller. The graphics are divided into "cells" 12 by 18 pixels in size. The cells are stored in an on-chip static RAM (4096 words by 24 bits) and can be stored as 1-bit per pixel data, 2-bit per pixel data or 4-bit per pixel data. This permits a good compression ratio while allowing more than 16 colors in the image.

4.13.1 On-Chip OSD SRAM

The on-chip static RAM (4096 words by 24 bits) stores the cell map and the cell definitions.

In memory, the cell map is organized as an array of words, each defining the attributes of one visible character on the screen starting from upper left of the visible character array. These attributes specify which character to display, whether it is stored as 1, 2 or 4 bits per pixel, the foreground and background colors, blinking, etc.

Registers CELLMAP_XSZ and CELLMAP_YSZ are used to define the visible area of the OSD image. For example, Figure 24 shows a cell map for which CELLMAP_XSZ =25 and CELLMAP_YSZ =10.

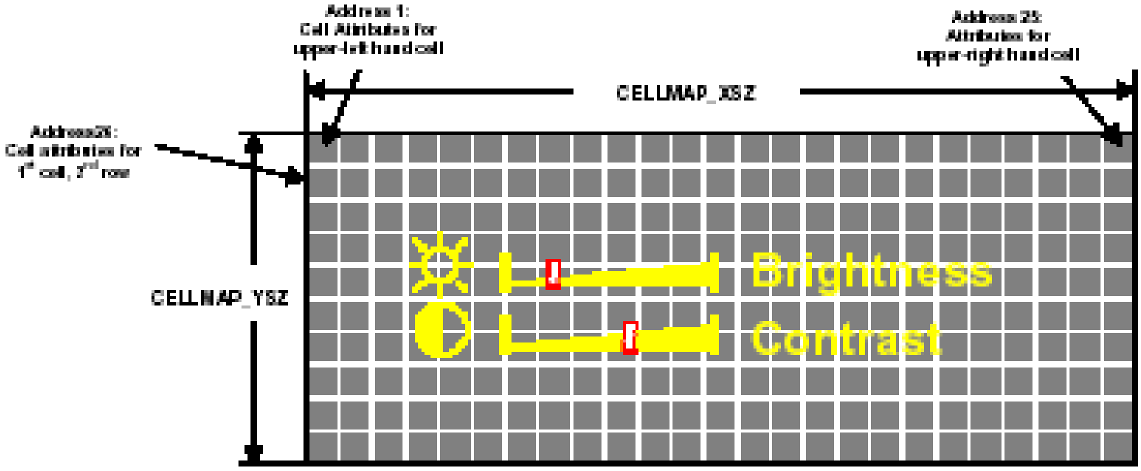


Figure 24. OSD Cell Map

Cell definitions are stored as bit map data. On-chip registers point to the start of 1-bit per pixel definitions, 2-bit per pixel definitions and 4-bit per pixel definitions respectively. 1, 2 and 4-bit per pixel cell definitions require 9, 18 and 36 words of the OSD RAM respectively.

Note that the cell map and the cell definitions share the same on-chip RAM. Thus, the size of the cell map can be traded off against the number of different cell definitions. In particular, the size of the OSD image and the number of cell definitions must fit in OSD SRAM. That is, the following inequality must be satisfied. (Note, the ROUND operation rounds 3.5 to 4).

(CELLMAP_XSZ+1) * CELLMAP_YSZ +
18 * ROUND(Number of 1-bit per pixel fonts / 2) +
18 * (Number of 2-bit per pixel fonts) +
36 * (Number of 4-bit per pixel fonts)   <= 4096

For example, an OSD menu 360 pixels wide by 360 pixels high is 30 cells in width and 20 cells in height. Many of these cells would be the same (e.g. empty). In this case, the menu could contain more than 32 1-bit per pixel cells, 100 2-bit per pixel cells, and 16 4-bit per pixel cells. Of course, different numbers of each type can also be used.

4.13.2 Color Look-up Table (LUT)

Each pixel of a displayed cell is resolved to an 8-bit color code. This selected color code is then transformed to a 24-bit value using a 256 x 24-bit look up table. This LUT is stored in an on-chip RAM that is separate from the OSD RAM. Color index value 0x00 is reserved for transparent OSD pixels.

4.13.3 OSD Position

The OSD menu can be positioned anywhere on the display region. The reference point is Horizontal and Vertical Display Background Start (DH_BKGND_START and DV_BKGND_START in Figure 18).

4.13.4 OSD Stretch

The OSD image can be stretched horizontally and/or vertically by a factor of two, three, or four. Pixel and line replication is used to stretch the image.

4.13.5 Blending

Sixteen levels of blending are supported for the character-mapped and bitmapped images. One host register controls the blend levels for pixels with LUT values of 128 and greater, while another host register controls the blend levels for pixels with LUT values of 127 and lower. OSD color LUT value 0 is reserved for transparency and is unaffected by the blend attribute.

Blend levels for binary codes "1111" through "0000" are 6.25%, 12.5%, 18.75%, 25%, 31.25%, 37.5%, 43.75%, 50%, 56.25%, 62.5%, 68.75%, 75%, 81.25%, 87.5%, 93.75%, 100%. Blend percentage level refers the percentage of the output data that is OSD.

4.14 On-Chip Microcontroller (OCM)

The gm5115/25 on-chip microcontroller (OCM) serves as the system microcontroller. It programs the gm5115/25 and manages other devices in the system such as the keypad, the back light and non-volatile RAM (NVRAM) using general-purpose input/output (GPIO) pins.

The OCM can operate in two configurations, Standalone configuration and Full-Custom configuration, as illustrated in Figure 25.

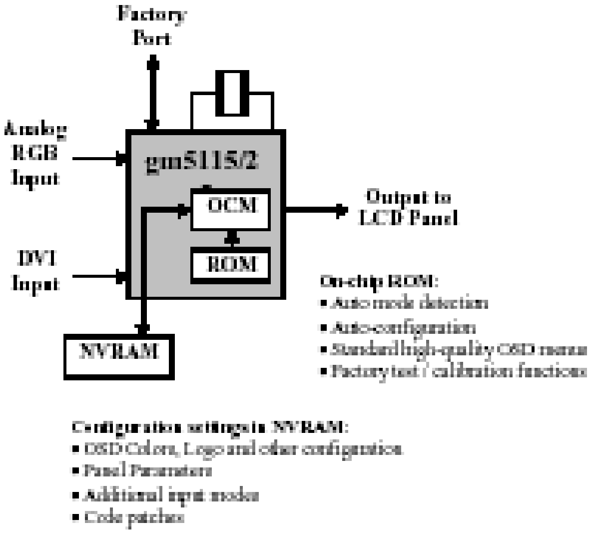


Figure 25A - Standalone Configuration

(No external ROM)

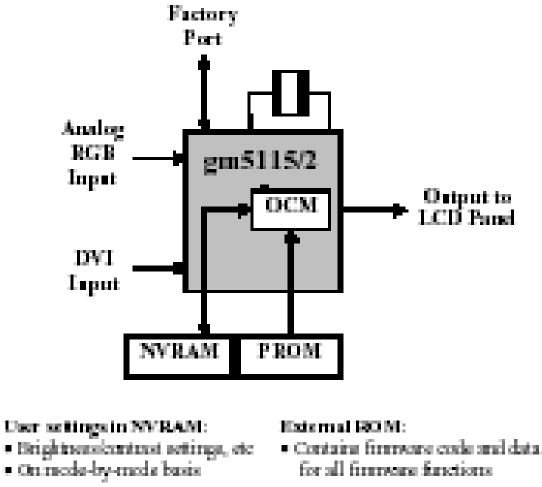


Figure 25B - Full-Custom Configuration

(Program and Data stored in external ROM)

4.14.1 Standalone Configuration

Standalone configuration offers the most simple and inexpensive system solution for generic LCD monitors. In this configuration the OCM executes firmware stored internally in gm5115/25. This is illustrated in Figure 25A. The on-chip firmware provides all the standard functions required in a high-quality generic LCD monitor. This includes mode-detection, auto-configuration and a high-quality standard OSD menu system. No external ROM is required (which reduces BOM cost) and no firmware development effort is required (which reduces time-to-market).

In Standalone configuration many customization parameters are stored in NVRAM. These include the LCD panel timing parameters (including TCON programming), the color scheme and logos used in the OSD menus, the functions provided by the OSD menus, and arbitrary firmware modifications. These customization parameters are described in the Standalone

User's Guide (B0108-SUG-01). Based on the customization parameters, G-Wizard (a GUI-based development tool used to program Genesis devices) produces the hex image file for NVRAM. G-Probe is then used to download the NVRAM image file into the NVRAM device. This is illustrated in Figure 26 below.

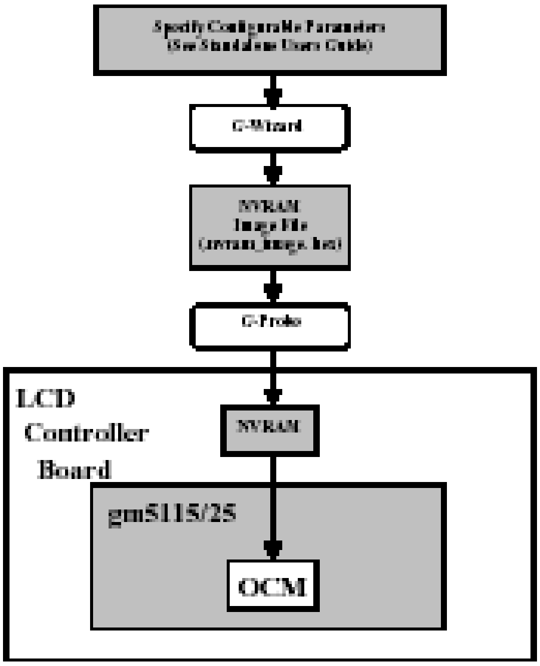


Figure 26. Programming OCM in Standalone Configuration

4.14.2 Full-Custom Configuration

In full-custom configuration the OCM executes a firmware program running from external ROM. This is illustrated in Figure 25B. A parallel port with separate address and data busses is available for this purpose. This port connects directly to standard, commercially available ROM or programmable Flash ROM devices. Normally 64KB or 128KB of ROM is required.

Both instructions and data are fetched from external ROM on a cycle-by-cycle basis. The speed of the accesses on the parallel port is determined by the gm5115/25 internal OCM_CLK. This in turn determines the speed of the external ROM device. For example, if a 14.3 MHz crystal is being used to produce TCLK, and the OCM_CLK is derived from TCLK, then a 45ns ROM can be used.

To program gm5115/25 in full-custom configuration the content of the external ROM is generated using Genesis software development tools G-Wizard and OSD-Workbench. This is illustrated in Figure 27. G-Wizard is a GUI-based tool for capturing system information such

as panel timing, support modes, system configuration, etc. OSD-Workbench is a GUI based tool for defining OSD menus and functionality.

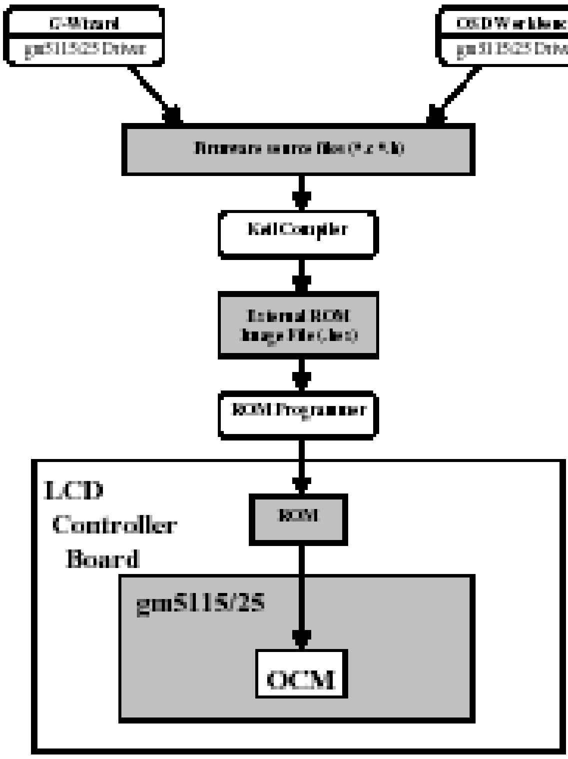


Figure 27. Programming the OCM in Full-Custom Configuration

Genesis recommends using Keil compiler (http://www.keil.com/) to compile the firmware source code into a hex file. This hex file is then downloaded into the external ROM using commercially available ROM programmers.

For development purposes it may be useful to use a ROM emulator. For example, a PROMJET ROM emulator can be used (http://www.emutec.com/pjetmain.html).

4.14.3 General Purpose Inputs and Outputs (GPIO)

The gm5115/25 has 21 general-purpose input/output (GPIO) pins. These are used by the OCM to communicate with other devices in the system such as keypad buttons, NVRAM, LEDs, audio DAC, etc. Each GPIO has independent direction control, open drain enable, for reading and writing. Note that the GPIO pins have alternate functionality as described in Table 17 below.

Pin Name	Pin Number	Alternate function
GPIO0/PWM0 GPIO1/PWM1 GPIO2/PWM2	40 41 42	PWM0, PWM1 and PWM2 back light intensity controls, as described in section 4.17.2 below.
GPIO3/TIMER1	43	Timer1 input of the OCM.
GPIO4/UART_DI GPIO5/UART_DO	44 45	OCM UART data in/out signals respectively.
GPIO6/TCON_SHC GPIO7/TCON_TDIV	46 47	Horizontal timing signals in the TCON column driver interface.
GPIO8/IRQINn	39	OCM external interrupt source (IRQINn).
GPIO9/TCON_ROE2 GPIO10/TCON_ROE3	48 49	Row output enables ROE2 and ROE3 in the TCON row driver interface.
GPIO11/ROM_WEn	50	Write enable for external ROM if programmable FLASH device is used.
GPIO12/NVRAM_SDA GPIO13/NVRAM_SCL	51 52	Data and clock lines for master 2-wire serial interface to NVRAM when gm5115/25 is used in standalone configuration (section Figure 25).
GPIO14/DDC_SCL GPIO15/DDC_SDA	6 7	Clock and data lines for 2-wire serial interface connected to the Direct Data Channel (DDC) of the DVI input, for passing HDCP keys.
GPIO16/HFSn	205	Serial data line for 2-wire host interface.
GPIO17 GPIO18 GPIO19 GPIO20	1 208 207 206	No alternative function.
GPIO21/IRQn	4	OCM interrupt output pin.
GPIO22/HCLK	204	Serial input clock for 2-wire host interface.

Table 17. gm5115/25 GPIOs and Alternate Functions

4.15 Bootstrap Configuration Pins

During hardware reset, the external ROM address pins ROM_ADDR[15:0] are configured as inputs. On the negating edge of RESETn, the value on these pins is latched and stored. This value is readable by the on-chip microcontroller (or an external microcontroller via the host interface). Install a 10K pull-up resistor to indicate a '1', otherwise a '0' is indicated.

Signal Name	Pin Name	Description
HOST_ADDR(4:0) USER_BITS(4:0)	ROM_ADDR(4:0)	If using 2-wire host protocol, these are bits 4:0 of the serial bus device address. Otherwise, these settings are available for reading from a status register but are otherwise unused by the gm5115/25. Used for "soft" configuration settings.
HOST_ADDR(5)	ROM_ADDR5	If using 2-wire host protocol, this is bit 5 of serial the bus device address. Otherwise, program this bit to 0.
HOST_ADDR(6)	ROM_ADDR6	If using 2-wire host protocol, this is bit 6 of the serial bus device address. Otherwise, program this bit to 0.
HOST_PROTOCOL	ROM_ADDR7	Program this bit to 0 for 2-wire host protocol operation.
HOST_PORT_EN	ROM_ADDR8	Program this bit to 0 for 2-wire host protocol operation.
OCM_START	ROM_ADDR9	Determines the operating condition of the OCM after HW reset: 0 = OCM remains in reset until enabled by register bit. 1 = OCM becomes active after OCM_CLK is stable.
USER_BITS(7:5)	ROM_ADDR(12:10)	These settings are available for reading from a status register but are otherwise unused by the gm5115/25.
OSC_SEL	ROM_ADDR13	Selects reference clock source: 0 = XTAL and TCLK pins are connected to a crystal oscillator (see Figure 4). 1 = TCLK input is driven with a single-ended TTL/CMOS clock oscillator (see Figure 7).
OCM_ROM_CNFG(1)	ROM_ADDR14	Together with OCM_CONTROL register (0x22) bit 4, this bit selects internal/external ROM configuration. 0 = All 48K of ROM is internal. 1 = All 48K of ROM is in external ROM using ROM_ADDR15:0 address outputs if register 0x22 bit 4 is 0. If register 0x22 bit 4 is 1, 0-32K ROM is internal, and 32K–48K ROM is external using ROM_ADDR15:0 address outputs.

Table 18. Bootstrap Signals

4.16 Host Interface

A serial host interface is provided to allow an external device to peek and poke registers in the gm5115/25. This is done using a 2-wire serial protocol. Note that 2-wire host interface requires bootstrap settings as described in Table 18.

The 2-wire host interface is suitable for connection to a factory interrogation port. This is illustrated in Figure 28. The factory test station connects to the gm5115/25 through the Direct Data Channel (DDC) of the DSUB15 or DVI connectors. For example, the PC can make gm5115/25 display test patterns (see section 4.5). A camera can be used to automate the calibration of the LCD panel.



Figure 28. Factory Calibration and Test Environment

An arbitration mechanism ensures that register accesses from the OCM and the 2-wire host interface port are always serviced (time division multiplexing).

4.16.1 Host Interface Command Format

Transactions on the 2-wire host protocol occurs in integer multiples of bytes (i.e. 8 bits or two nibbles respectively). These form an instruction byte, a device register address and/or one or more data bytes. This is described in Table 19.

The first byte of each transfer indicates the type of operation to be performed by the gm5115/25. The table below lists the instruction codes and the type of transfer operation. The content of bytes that follow the instruction byte will vary depending on the instruction chosen. By utilizing these modes effectively, registers can be quickly configured.

The two LSBs of the instruction code, denoted 'A9' and 'A8' in Table 19 below, are bits 9 and 8 of the internal register address respectively. Thus, they should be set to '00' to select a starting register address of less than 256, '01' to select an address in the range 256 to 511, and '10' to select an address in the range 512 to 767. These bits of the address increment in Address Increment transfers. The unused bits in the instruction byte, denoted by 'x', should be set to '1'.

Table 19. Instruction Byte Map

Bit 7 6 5 4 3 2 1 0	Operation Mode	Description
0 0 0 1 x x A9 A8	Write Address Increment	Allows the user to write a single or multiple bytes to a specified starting address location. A Macro operation will cause the internal address pointer to increment after each byte transmission. Termination of the transfer will cause the address pointer to increment to the next address location.
0 0 1 0 x x A9 A8	Write Address No Increment (for table loading)	
1 0 0 1 x x A9 A8	Reserved	Allows the user to read multiple bytes from a specified starting address location. A Macro operation will cause the internal address pointer to increment after each read byte. Termination of the transfer will cause the address pointer to increment to the next address location.
1 0 1 0 x x A9 A8	Read Address No Increment (for table reading)	
0 0 1 1 x x A9 A8 0 1 0 0 x x A9 A8 1 0 0 0 x x A9 A8 1 0 1 1 x x A9 A8 1 1 0 0 x x A9 A8	Reserved	
0 0 0 0 x x A9 A8 0 1 0 1 x x A9 A8 0 1 1 0 x x A9 A8 0 1 1 1 x x A9 A8 1 1 0 1 x x A9 A8 1 1 1 0 x x A9 A8 1 1 1 1 x x A9 A8	Spare	No operation will be performed

4.16.2 2-wire Serial Protocol

The 2-wire protocol consists of a serial clock HCLK (pin number 204) and bi-directional serial data line HFSn (pin number 205). The bus master drives HCLK and either the master or slave can drive the HFSn line (open drain) depending on whether a read or write operation is being performed. The gm5115/25 operates as a slave on the interface.

The 2-wire protocol requires each device be addressable by a 7-bit identification number. The gm5115/25 is initialized on power-up to 2-wire mode by asserting bootstrap pins HOST_PROTOCOL=0 and the device identification number on HOST_ADDR(6:0) on the rising edge of RESETn (see Table 18). This provides flexibility in system configuration with multiple devices that can have the same address.

A 2-wire data transfer consists of a stream of serially transmitted bytes formatted as shown in the figure below. A transfer is initiated (START) by a high-to-low transition on HFSn while HCLK is held high. A transfer is terminated by a STOP (a low-to-high transition on HFSn while HCLK is held high) or by a START (to begin another transfer). The HFSn signal must be stable when HCLK is high, it may only change when HCLK is low (to avoid being misinterpreted as START or STOP).



Figure 29. 2-Wire Protocol Data Transfer

Each transaction on the HFSn is in integer multiples of 8 bits (i.e. bytes). The number of bytes that can be transmitted per transfer is unrestricted. Each byte is transmitted with the most significant bit (MSB) first. After the eight data bits, the master releases the HFSn line and the receiver asserts the HFSn line low to acknowledge receipt of the data. The master device generates the HCLK pulse during the acknowledge cycle. The addressed receiver is obliged to acknowledge each byte that has been received.

The Write Address Increment and the Write Address No Increment operations allow one or multiple registers to be programmed with only sending one start address. In Write Address Increment, the address pointer is automatically incremented after each byte has been sent and written. The transmission data stream for this mode is illustrated in Figure 30 below. The highlighted sections of the waveform represent moments when the transmitting device must release the HFSn line and wait for an acknowledgement from the gm5115/25 (the slave receiver).

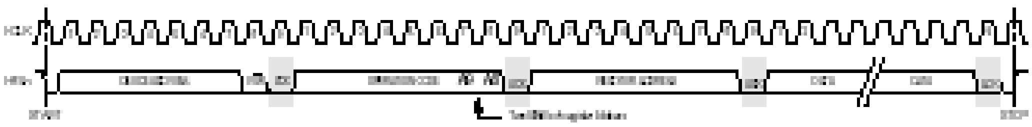


Figure 30. 2-Wire Write Operations (0x1x & 0x2x)

The Read Address No Increment (0xA0) operation is illustrated in Figure 31. The highlighted sections of the waveform represent moments when the transmitting device must release the HFSn line and waits for an acknowledgement from the master receiver.

Note that on the last byte read, no acknowledgement is issued to terminate the transfer.

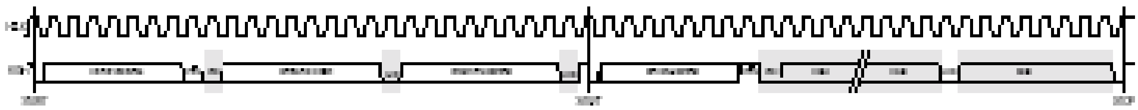


Figure 31. 2-Wire Read Operation (0xAx)

Please note that in all the above operations the operation code includes two address bits, as described in Table 19.

4.17 Miscellaneous Functions

4.17.1 Power Down Operation

The gm5115/25 provides a low power state in which the clocks to selected parts of the chip may be disabled (see Table 21).

4.17.2 Pulse Width Modulation (PWM) Back Light Control

Many of today's LCD back light inverters require both a PWM input and variable DC voltage to minimize flickering (due to the interference between panel timing and inverter's AC timing), and adjust brightness. Most LCD monitor manufacturers currently use a microcontroller to provide these control signals. To minimize the burden on the external microcontroller, the gm5115/25 generates these signals directly.

There are three pins available for controlling the LCD back light, PWM0 (GPIO0), PWM1 (GPIO1) and PWM2 (GPIO2). The duty cycle of these signals is programmable. They may be connected to an external RC integrator to generate a variable DC voltage for a LCD back light inverter. Panel HSYNC is used as the clock for a counter generating this output signal.

5. ELECTRICAL SPECIFICATIONS

The following targeted specifications have been derived by simulation.

5.1 Preliminary DC Characteristics

Table 20. Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
3.3V Supply Voltages [1]	$V_{VDD_3.3}$	-0.3		3.6	V
2.5V Supply Voltages [1]	$V_{VDD_2.5}$	-0.3		2.75	V
Input Voltage (5V tolerant inputs) [1]	$V_{IN5Vtol}$	-0.3		5.5	V
Input Voltage (non 5V tolerant inputs) [1]	V_{IN}	-0.3		3.6	V
Electrostatic Discharge	V_{ESD}			±2.0	kV
Latch-up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		125	°C
Operating Junction Temp.	T_J	0		125	°C
Thermal Resistance (Junction to Air) Natural Convection XGA SXGA	 θ_{JA_XGA} θ_{JA_SXGA}			 25.0 TBD	°C/W
Thermal Resistance (Junction to Case) Convection or air flow XGA SXGA	 θ_{JC_XGA} θ_{JC_SXGA}			 14.0 TBD	°C/W
Soldering Temperature (30 sec.)	T_{SOL}			220	°C
Vapor Phase Soldering (30 sec.)	T_{VAP}			220	°C

NOTE: All voltages are measured with respect to GND

NOTE (1): Absolute maximum voltage ranges are for transient voltage excursions.

NOTE (2): Package thermal resistance is based on a PCB with one signal plane and two power planes. Package θ_{JA} is improved on a PCB with four or more layers.

Table 21. DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
POWER					
Power Consumption @ 96 MHz (gm5115)	P_{XGA}		1.8		W
Power Consumption @ 135 MHz (gm5125)	P_{XGA}		2.2		W
Power Consumption @ Low Power Mode [1]	P_{LP}		0.5		W
3.3V Supply Voltages (AVDD and RVDD)	$V_{VDD_3.3}$	3.15	3.3	3.45	V
2.5V Supply Voltages (VDD and CVDD)	$V_{VDD_2.5}$	2.35	2.5	2.65	V
Supply Current @ CLK = 96 MHz (gm5115) • 2.5V digital supply [2] • 2.5V analog supply [3] • 3.3V digital supply [4] • 3.3V analog supply [5]	I_{XGA} $I_{XGA_2.5_VDD}$ $I_{XGA_2.5_AVDD}$ $I_{XGA_3.3_VDD}$ $I_{XGA_3.3_AVDD}$		400	 360 40 50 150	mA
Supply Current @ CLK =135MHz (gm5125) • 2.5V digital supply [2] • 2.5V analog supply [3] • 3.3V digital supply [4] • 3.3V analog supply [5]	I_{XGA} $I_{XGA_2.5_VDD}$ $I_{XGA_2.5_AVDD}$ $I_{XGA_3.3_VDD}$ $I_{XGA_3.3_AVDD}$			 540 50 60 150	mA
Supply Current @ Low Power Mode*	I_{LP}		140		mA
INPUTS					
High Voltage	V_{IH}	2.0		V_{DD}	V
Low Voltage	V_{IL}	GND		0.8	V
Clock High Voltage	V_{IHC}	2.4		V_{DD}	V
Clock Low Voltage	V_{ILC}	GND		0.4	V
High Current (V_{IN} = 5.0 V)	I_{IH}	-25		25	µA
Low Current (V_{IN} = 0.8 V)	I_{IL}	-25		25	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}			8	pF
OUTPUTS					
High Voltage (I_{OH} = 7 mA)	V_{OH}	2.4		V_{DD}	V
Low Voltage (I_{OL} = -7 mA)	V_{OL}	GND		0.4	V
Tri-State Leakage Current	I_{OZ}	-25		25	µA

NOTE (1): Low power figures result from setting the ADC, TMDS, and clock power down bits.
NOTE (2): Includes pins CVDD_2.5, VDD1_ADC_2.5, VDD2_ADC_2.5, VDD_RX0_2.5, VDD_RX1_2.5 and VDD_RX2_2.5.
NOTE (3): Includes only VDD_RXPLL_2.5.
NOTE (4): Includes pins VDD_DPLL, VDD_SDDS, VDD_DDDS and RVDD.
NOTE (5): Includes pins AVDD_RED, AVDD_GREEN, AVDD_BLUE, AVDD_IMB, AVDD_RX0, AVDD_RX1, AVDD_RX2, AVDD_RXC, AVDD_RPLL, AVDD_SDDS and AVDD_DDDS.

5.2 Preliminary AC Characteristics

The following targeted specifications have been derived by simulation.

All timing is measured to a 1.5V logic-switching threshold. The minimum and maximum operating conditions used were: T_{DIE} = 0 to 125° C, Vdd = 2.35 to 2.65V, Process = best to worst, C_L = 16pF for all outputs.

Table 22. Maximum Speed of Operation

Clock Domain	Max Speed of Operation
Main Input Clock (TCLK)	24 MHz (14.3MHz recommended)
TMDS Differential Input Clock	165 MHz
ADC Clock (ACLK)	162.5 MHz
HCLK Host Interface Clock (2-wire protocol)	5 MHz
Input Format Measurement Clock (IFM_CLK)	50MHz (14.3MHz recommended)
Reference Clock (RCLK)	200MHz (200MHz recommended)
On-Chip Microcontroller Clock (OCM_CLK)	100 MHz
Display Clock (DCLK)	135 MHz

Table 23. Display Timing and DCLK Adjustments

DP_TIMING ->	Tap 0 (default)		Tap 1		Tap 2		Tap 3	
	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Propagation delay from DCLK to DA*/DB*	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5
Propagation delay from DCLK to DHS	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5
Propagation delay from DCLK to DVS	0.5	4.5	0.0	3.5	-1.0	2.5	-2.0	1.5
Propagation delay from DCLK to DEN	1.0	4.5	0.5	3.5	-0.5	2.5	-1.5	1.5

Note: DCLK Clock Adjustments are the amount of additional delay that can be inserted in the DCLK path, in order to reduce the propagation delay between DCLK and its related signals.

Table 24. 2-Wire Host Interface Port Timing

Parameter	Symbol	MIN	TYP	MAX	Units
SCL HIGH time	T_{SHI}	1.25			us
SCL LOW time	T_{SLO}	1.25			us
SDA to SCL Setup	T_{SDIS}	30			ns
SDA from SCL Hold	T_{SDIH}	20			ns
Propagation delay from SCL to SDA	T_{SDO}	10		150	ns

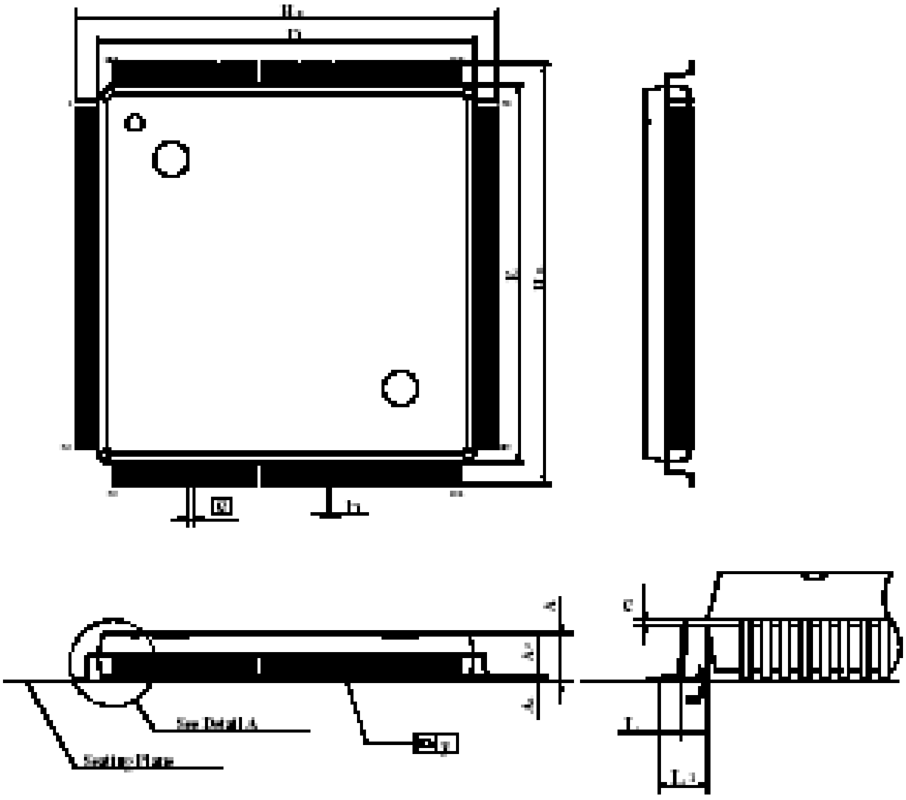
Note: The above table assumes OCM_CLK = R_CLK / 2 = 100 MHz (default) (ie 10ns / clock)

6. ORDERING INFORMATION

Order Code	Application	Package	Speed	Temperature Range
gm5115	XGA	208-pin PQFP	96 MHz	0-70°C
gm5125	SXGA	208-pin PQFP	135 MHz	0-70°C

7. MECHANICAL SPECIFICATIONS

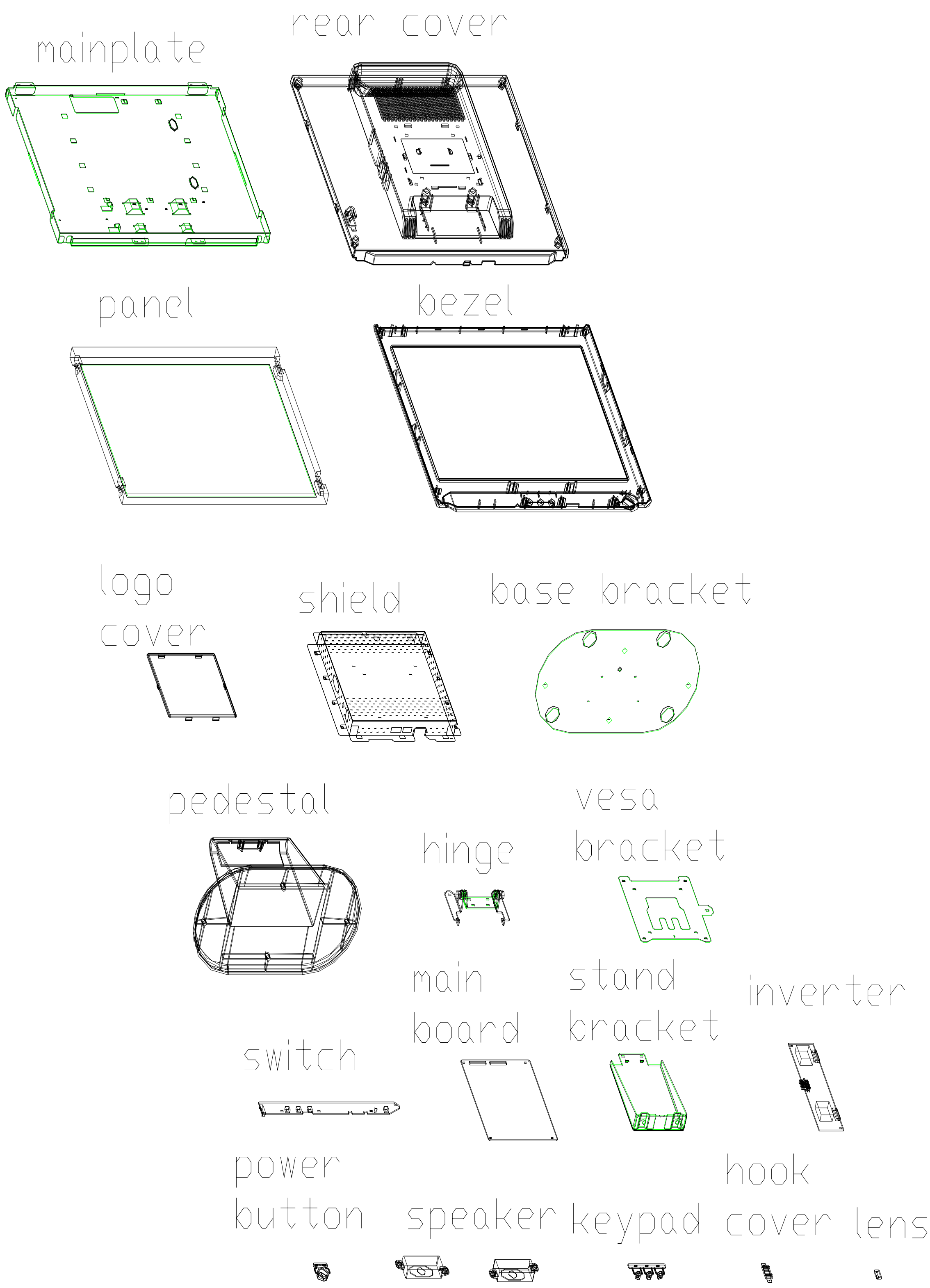
Figure 32. gm5115/25 208-pin PQFP Mechanical Drawing



Detail A

Symbol	Dimension in mm		
	Min	Nom	Max
A	3.60	—	4.07
A_1	0.25	—	—
A_2	3.18	3.32	3.38
b	0.18	—	0.28
c	0.10	—	0.23
D	27.90	28.00	28.10
E	27.90	28.00	28.10
e	0.50 BSC		
H_D	30.90	31.20	31.40
H_E	30.90	31.20	31.40
L	0.65	0.88	1.03
L_1	1.60 REF		
y	—	—	0.10
θ	0°	—	7°

7. MECHANICAL OF CABINET FRONT DIS-ASSEMBLY



8.PARTS LISTING

1.FT5017 FOR HANNSTAR*83 PANEL

PARTS LIST OF CABINET

LOCATION	TF1562-S3	SPECIFICATION
	CBPC560KHDC3	CONVERSION BOARD FOR T5
	KEPC560KB1	KEY BOARD FOR T563K*COM
	7L 1 L 6	刺314
	15L5689 2 A	GND CLAMP
	15L5753 1	MAIN BRACKET
	33L4438 A6 T	LOGO COVER
	40L 150716 2A	ID LABEL
	40L 152509	RECYCLE LABEL
	40L 152512	RECYCLE LABEL
	40L 154 14 1	CABINET LABEL
	40L 457716 1A	TCO99 LABEL
	40L 581 26704	酮襛 FOR CARTON/PALLET
	40L 581716 1A	CARTON LABEL
	41L 68508 A	恨
	41L1500716 4B	DOC KIT(272943-292)
	44L3231 15	EVA WASHER
	44L3231501	旧篆�titsmith粗
	44L3231506	旧篆猸粗
	44L3510 1EPE	EPE-R
	44L3510 2EPE	EPE-L
	44L3510 5	U TYPE PAPER SHEET
	44L3510716 4B	CARTON
	44L9003 9	CORNER PAPER
	45L 77 3	ゴ 饯
	45L 77500	BARCODE RIBBON
	45L 77501	BARCODE RIBBON
	45L 88607 CP	PE BAG
	45L 88609	EPE COVER
	52L 1185 16	MIDDLE TAPE
	52L 1186	SMALL TAPE
	52L6020 2	PROTECT FILM
	52L6021 3	荡粲
	71L 100 19	WS ZP 5*12*25
	79L L15 12 E	INVERTER BY EMAX
	80L L15 11 LS	ADAPTOR BY LINE SHIN
	80L L15 11 LT	ADAPTER
	85L 601 1	SHIELD CASE
	89L 173L15 28	SIGNAL CABLE
	89L 176 40 2	FFC CABLE 40P 50mm
	89L401A18NISB	POWER CORD

	M1L 330 4128	SCREW M3X4
	M1L 330 6128	SCREW
	M1L1030 12128	SCREW M3X12
	M1L1740 10 47	SCREW M4X10
	Q1L1030 8 47	SCREW 3mmX8
	Q1L1030 10128	SCREW
	705L563KB34002	LCD 催 ASS'Y
	750LLH50X83	HANNSTAR 15" S.I PANEL

PARTS LIST OF BACK COVER ASS'Y

LOCATION	705L563KB34002	SPECIFICATION
	12L 387 2	RUBBER FOOT
	15L5752 1	BASE BRACKET
	15L5754 1	VESA BRACKET
	15L5755 1	STAND BRACKET
	33L4434 1	LENS
	33L4435 A5 L	KEY PAD
	33L4436 A7 L	POWER BUTTON
	33L4439 A6 L	HOOL COVER
	34L 968AA5 T	FRONT PANEL
	34L 970AA6 1T	BACK COVER
	34L 971 A6 B	PEDESTAL
	37L 456 1	HINGE
	M1L1740 8128	SCREW M4X8
	Q1L 340 10128	SCREW 4X10mm
	CQ1L 140 8128	SCREW

PARTS LIST OF CONVERSION BOARD

LOCATION	CBPC560KHDC3	SPECIFICATION
	AI560KHDC3	CBPC AUTO INS. FOR T563
CN5	33L3802 7	WAFER EH-7
CN6	33L8022 6A H	HEADER FEMALE 6P
	49L 51 1A	簕猳
	55L 100600 A	ň 盼瞜奎
	55L 100603	κ て瞜奎
U5	56L1133 35 H1	W49F 002UP
C101	67L 305331 4	330UF +-20% 25V
C79	67L 305331 4	330UF +-20% 25V
C95	67L 305331 4	330UF +-20% 25V
L5	71L 55 28	FERRITE BEAD 7.62*5.08*
CN12	88L 304 8K	DC POWER JACK SCD-014A
CN1	88L 35315F HS	D-SUB 15PIN FEMALE
X1	93L 22 53	CRYSTAL 14.318MHzHC-49U

PARTS LIST OF CONVERSION BOARD AUTO INSERTION

LOCATION	AI560KHDC3	SPECIFICATION
CN3	33L8019 40	CONNECTOR 40P SMT
CN4	33L8019 40	CONNECTOR 40P SMT
	55L 23520	IPA
	55L 100600 A	ň 聆瞜奎
	55L 100602	奎籌
U3	56L 562 17	GM2115
U7	56L 585 4	AIC1117-33CY SMT
U9	56L 585 5	RT9164-25CG
U10	56L 622 1	BA9741F-SMT
U6	56L1133 33	M24C16-MN6T SMT
U1	56L1133 34	M24C02-WMN6T SMT
U2	56L4LVC 14 F	74LVC14 BY FAIRCHILD
U2	56L4LVC 14 P	74LVC14ADT
Q2	57L 417 4	PMBS3904/PHILIPS-SMT
Q3	57L 417 4	PMBS3904/PHILIPS-SMT
Q6	57L 417 4	PMBS3904/PHILIPS-SMT
Q5	57L 417 6	PMBS3906/PHILIPS-SMT
Q8	57L 417 6	PMBS3906/PHILIPS-SMT
Q1	57L 763 1	A03401 SOT23 BY AO
Q4	57L 763 2	AO4403 SO-8 BY AOS SMT
Q7	57L 763 2	AO4403 SO-8 BY AOS SMT
RP4	61L 125103 8	CHIP AR 8P4R 10KOHM +-5
RP6	61L 125472 8	CHIP AR 8P4R 4.7K OHM+-
R57	61L0603100	CHIP 10 OHM 1/16W
R1	61L0603101	CHIPR 100 OHM +-5% 1/16
R2	61L0603101	CHIPR 100 OHM +-5% 1/16
R5	61L0603101	CHIPR 100 OHM +-5% 1/16
R6	61L0603101	CHIPR 100 OHM +-5% 1/16
R60	61L0603101	CHIPR 100 OHM +-5% 1/16
R71	61L0603101	CHIPR 100 OHM +-5% 1/16
R8	61L0603101	CHIPR 100 OHM +-5% 1/16
R9	61L0603101	CHIPR 100 OHM +-5% 1/16
R29	61L0603102	CHIPR 1K OHM +-5% 1/16W
R37	61L0603102	CHIPR 1K OHM +-5% 1/16W
R54	61L0603102	CHIPR 1K OHM +-5% 1/16W
R70	61L0603102	CHIPR 1K OHM +-5% 1/16W
R14	61L0603103	CHIPR 10K OHM +-5% 1/16
R3	61L0603103	CHIPR 10K OHM +-5% 1/16
R30	61L0603103	CHIPR 10K OHM +-5% 1/16
R31	61L0603103	CHIPR 10K OHM +-5% 1/16
R35	61L0603103	CHIPR 10K OHM +-5% 1/16
R36	61L0603103	CHIPR 10K OHM +-5% 1/16
R38	61L0603103	CHIPR 10K OHM +-5% 1/16
R39	61L0603103	CHIPR 10K OHM +-5% 1/16

R4	61L0603103	CHIPR 10K OHM +-5% 1/16
R40	61L0603103	CHIPR 10K OHM +-5% 1/16
R45	61L0603103	CHIPR 10K OHM +-5% 1/16
R68	61L0603103	CHIPR 10K OHM +-5% 1/16
R73	61L0603103	CHIPR 10K OHM +-5% 1/16
R78	61L0603103	CHIPR 10K OHM +-5% 1/16
R79	61L0603103	CHIPR 10K OHM +-5% 1/16
R43	61L0603104	CHIPR 100K OHM +-5% 1/1
R65	61L0603123	CHIP 12K OHM 1/16W
R61	61L0603183	CHIP 18K OHM 1/16W
R69	61L0603183	CHIP 18K OHM 1/16W
R16	61L0603202	CHIPR 2K OHM+-5% 1/16W
R17	61L0603202	CHIPR 2K OHM+-5% 1/16W
R62	61L0603203	CHIPR 20K OHM+-5% 1/16W
R41	61L0603221	CHIPR 220 OHM+-5% 1/16W
R42	61L0603221	CHIPR 220 OHM+-5% 1/16W
R24	61L0603272	CHIP 2.7K OHM 1/16W
R76	61L0603301	CHIP 300 OHM 1/16W
R77	61L0603301	CHIP 300 OHM 1/16W
R58	61L0603303	CHIP 30K OHM 5% 1/16W
R63	61L0603303	CHIP 30K OHM 5% 1/16W
R72	61L0603303	CHIP 30K OHM 5% 1/16W
R10	61L0603470	CHIPR 47 OHM +-5% 1/16W
R18	61L0603470	CHIPR 47 OHM +-5% 1/16W
R19	61L0603470	CHIPR 47 OHM +-5% 1/16W
R7	61L0603470	CHIPR 47 OHM +-5% 1/16W
R15	61L0603472	CHIPR 4.7K OHM +-5% 1/1
R23	61L0603472	CHIPR 4.7K OHM +-5% 1/1
R25	61L0603472	CHIPR 4.7K OHM +-5% 1/1
R32	61L0603472	CHIPR 4.7K OHM +-5% 1/1
R33	61L0603472	CHIPR 4.7K OHM +-5% 1/1
R44	61L0603472	CHIPR 4.7K OHM +-5% 1/1
R56	61L0603473	CHIP 47K OHM 1/16W
R59	61L0603473	CHIP 47K OHM 1/16W
R64	61L0603473	CHIP 47K OHM 1/16W
R67	61L0603473	CHIP 47K OHM 1/16W
R55	61L0603563	CHIP 56K OHM 1/16W
R66	61L0603563	CHIP 56K OHM 1/16W
R11	61L0603750 9F	75OHM 1%
R12	61L0603750 9F	75OHM 1%
R13	61L0603750 9F	75OHM 1%
CP1	65L 600220 8T	22PF+-10% 50V 8P NPO SM
CP10	65L 600220 8T	22PF+-10% 50V 8P NPO SM
CP2	65L 600220 8T	22PF+-10% 50V 8P NPO SM
CP3	65L 600220 8T	22PF+-10% 50V 8P NPO SM
CP4	65L 600220 8T	22PF+-10% 50V 8P NPO SM
CP5	65L 600220 8T	22PF+-10% 50V 8P NPO SM
CP6	65L 600220 8T	22PF+-10% 50V 8P NPO SM

CP7	65L 600220 8T	22PF+-10% 50V 8P NPO SM
CP8	65L 600220 8T	22PF+-10% 50V 8P NPO SM
CP9	65L 600220 8T	22PF+-10% 50V 8P NPO SM
C105	65L0603102 32	CHIP 1000PF 50V X7R
C106	65L0603102 32	CHIP 1000PF 50V X7R
C107	65L0603102 32	CHIP 1000PF 50V X7R
C108	65L0603102 32	CHIP 1000PF 50V X7R
C109	65L0603102 32	CHIP 1000PF 50V X7R
C110	65L0603102 32	CHIP 1000PF 50V X7R
C117	65L0603102 32	CHIP 1000PF 50V X7R
C121	65L0603102 32	CHIP 1000PF 50V X7R
C122	65L0603102 32	CHIP 1000PF 50V X7R
C125	65L0603102 32	CHIP 1000PF 50V X7R
C62	65L0603102 32	CHIP 1000PF 50V X7R
C75	65L0603102 32	CHIP 1000PF 50V X7R
C86	65L0603102 32	CHIP 1000PF 50V X7R
C90	65L0603102 32	CHIP 1000PF 50V X7R
C1	65L0603103 32	0.01UF+-10% 50V X7R
C2	65L0603103 32	0.01UF+-10% 50V X7R
C4	65L0603103 32	0.01UF+-10% 50V X7R
C5	65L0603103 32	0.01UF+-10% 50V X7R
C6	65L0603103 32	0.01UF+-10% 50V X7R
C7	65L0603103 32	0.01UF+-10% 50V X7R
C76	65L0603103 32	0.01UF+-10% 50V X7R
C85	65L0603103 32	0.01UF+-10% 50V X7R
C89	65L0603103 32	0.01UF+-10% 50V X7R
C10	65L0603104 12	0.1UF +-10% 16V X7R
C102	65L0603104 12	0.1UF +-10% 16V X7R
C13	65L0603104 12	0.1UF +-10% 16V X7R
C14	65L0603104 12	0.1UF +-10% 16V X7R
C15	65L0603104 12	0.1UF +-10% 16V X7R
C16	65L0603104 12	0.1UF +-10% 16V X7R
C18	65L0603104 12	0.1UF +-10% 16V X7R
C19	65L0603104 12	0.1UF +-10% 16V X7R
C20	65L0603104 12	0.1UF +-10% 16V X7R
C21	65L0603104 12	0.1UF +-10% 16V X7R
C22	65L0603104 12	0.1UF +-10% 16V X7R
C23	65L0603104 12	0.1UF +-10% 16V X7R
C24	65L0603104 12	0.1UF +-10% 16V X7R
C25	65L0603104 12	0.1UF +-10% 16V X7R
C26	65L0603104 12	0.1UF +-10% 16V X7R
C27	65L0603104 12	0.1UF +-10% 16V X7R
C28	65L0603104 12	0.1UF +-10% 16V X7R
C3	65L0603104 12	0.1UF +-10% 16V X7R
C32	65L0603104 12	0.1UF +-10% 16V X7R
C33	65L0603104 12	0.1UF +-10% 16V X7R
C34	65L0603104 12	0.1UF +-10% 16V X7R
C35	65L0603104 12	0.1UF +-10% 16V X7R

C36	65L0603104 12	0.1UF +-10% 16V X7R
C37	65L0603104 12	0.1UF +-10% 16V X7R
C38	65L0603104 12	0.1UF +-10% 16V X7R
C39	65L0603104 12	0.1UF +-10% 16V X7R
C40	65L0603104 12	0.1UF +-10% 16V X7R
C41	65L0603104 12	0.1UF +-10% 16V X7R
C42	65L0603104 12	0.1UF +-10% 16V X7R
C43	65L0603104 12	0.1UF +-10% 16V X7R
C44	65L0603104 12	0.1UF +-10% 16V X7R
C46	65L0603104 12	0.1UF +-10% 16V X7R
C47	65L0603104 12	0.1UF +-10% 16V X7R
C48	65L0603104 12	0.1UF +-10% 16V X7R
C49	65L0603104 12	0.1UF +-10% 16V X7R
C50	65L0603104 12	0.1UF +-10% 16V X7R
C52	65L0603104 12	0.1UF +-10% 16V X7R
C56	65L0603104 12	0.1UF +-10% 16V X7R
C57	65L0603104 12	0.1UF +-10% 16V X7R
C58	65L0603104 12	0.1UF +-10% 16V X7R
C60	65L0603104 12	0.1UF +-10% 16V X7R
C64	65L0603104 12	0.1UF +-10% 16V X7R
C67	65L0603104 12	0.1UF +-10% 16V X7R
C77	65L0603104 12	0.1UF +-10% 16V X7R
C84	65L0603104 12	0.1UF +-10% 16V X7R
C88	65L0603104 12	0.1UF +-10% 16V X7R
C96	65L0603104 12	0.1UF +-10% 16V X7R
C97	65L0603104 12	0.1UF +-10% 16V X7R
C98	65L0603104 12	0.1UF +-10% 16V X7R
C92	65L0603105 17	1UF 16V Y5V
C93	65L0603105 17	1UF 16V Y5V
C94	65L0603105 17	1UF 16V Y5V
C128	65L0603220 31	CHIP 22PF 50V NPO
C129	65L0603220 31	CHIP 22PF 50V NPO
C130	65L0603220 31	CHIP 22PF 50V NPO
C131	65L0603220 31	CHIP 22PF 50V NPO
C132	65L0603220 31	CHIP 22PF 50V NPO
C133	65L0603220 31	CHIP 22PF 50V NPO
C8	65L0603470 32	CHIP 47PF 50V X7R
C9	65L0603470 32	CHIP 47PF 50V X7R
C99	65L0603471 32	CHIP 470PF 50V X7R
C100	65L0603473 32	CHIP 0.047UF 50V X7R
C91	65L0603473 32	CHIP 0.047UF 50V X7R
C53	65L0603509 31	CHIP 5PF+-0.5PF 50V NPO
C55	65L0603509 31	CHIP 5PF+-0.5PF 50V NPO
CP1	65L602K220 8T	IRRAY CAP 22PF +-10% 16
CP10	65L602K220 8T	IRRAY CAP 22PF +-10% 16
CP2	65L602K220 8T	IRRAY CAP 22PF +-10% 16
CP3	65L602K220 8T	IRRAY CAP 22PF +-10% 16
CP4	65L602K220 8T	IRRAY CAP 22PF +-10% 16

CP5	65L602K220 8T	IRRAY CAP 22PF +-10% 16
CP6	65L602K220 8T	IRRAY CAP 22PF +-10% 16
CP7	65L602K220 8T	IRRAY CAP 22PF +-10% 16
CP8	65L602K220 8T	IRRAY CAP 22PF +-10% 16
CP9	65L602K220 8T	IRRAY CAP 22PF +-10% 16
C12	67L 312100 3	SMD 10uf +-20% 16V
C30	67L 312100 3	SMD 10uf +-20% 16V
C51	67L 312100 3	SMD 10uf +-20% 16V
C54	67L 312100 3	SMD 10uf +-20% 16V
C61	67L 312100 3	SMD 10uf +-20% 16V
C59	67L 312101 3	SMD 100UF +-20% 16V
C11	67L 312470 3	SMD EC 47UF 16V +-20%
C17	67L 312470 3	SMD EC 47UF 16V +-20%
C29	67L 312470 3	SMD EC 47UF 16V +-20%
C31	67L 312470 3	SMD EC 47UF 16V +-20%
C45	67L 312470 3	SMD EC 47UF 16V +-20%
C63	67L 312470 3	SMD EC 47UF 16V +-20%
C66	67L 312470 3	SMD EC 47UF 16V +-20%
C83	67L 312470 3	SMD EC 47UF 16V +-20%
C87	67L 312470 3	SMD EC 47UF 16V +-20%
RP1	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP10	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP11	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP12	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP2	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP3	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP5	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP7	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP8	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP9	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
FB1	71L 56Z601	CHIP BEAD 600 OHM 0805
FB2	71L 56Z601	CHIP BEAD 600 OHM 0805
FB3	71L 56Z601	CHIP BEAD 600 OHM 0805
FB4	71L 56Z601	CHIP BEAD 600 OHM 0805
FB5	71L 56Z601	CHIP BEAD 600 OHM 0805
FB6	71L 56Z601	CHIP BEAD 600 OHM 0805
R20	71L 59B121	TB160808B12 SMD
R21	71L 59B121	TB160808B12 SMD
R22	71L 59B121	TB160808B12 SMD
R26	71L 59B121	TB160808B12 SMD
R27	71L 59B121	TB160808B12 SMD
R28	71L 59B121	TB160808B12 SMD
R20	71L 59C121 B	FCM1608C-121T03 SMD
R21	71L 59C121 B	FCM1608C-121T03 SMD
R22	71L 59C121 B	FCM1608C-121T03 SMD
R26	71L 59C121 B	FCM1608C-121T03 SMD
R27	71L 59C121 B	FCM1608C-121T03 SMD
R28	71L 59C121 B	FCM1608C-121T03 SMD

L3	73L 253136 TE	CHOKE COIL BY TECSTAR
L4	73L 253136 TE	CHOKE COIL BY TECSTAR
U5	87L 202 32	PLCC CONN 32PIN
ZD1	93L 39146	LL5232B SMT
ZD2	93L 39146	LL5232B SMT
ZD3	93L 39146	LL5232B SMT
ZD4	93L 39146	LL5232B SMT
ZD5	93L 39146	LL5232B SMT
ZD6	93L 39146	LL5232B SMT
ZD1	93L 39147	TZMC5V6-GS08 SMT
ZD2	93L 39147	TZMC5V6-GS08 SMT
ZD3	93L 39147	TZMC5V6-GS08 SMT
ZD4	93L 39147	TZMC5V6-GS08 SMT
ZD5	93L 39147	TZMC5V6-GS08 SMT
ZD6	93L 39147	TZMC5V6-GS08 SMT
ZD1	93L 39149	MLL5232B BY FULL POWER
ZD2	93L 39149	MLL5232B BY FULL POWER
ZD3	93L 39149	MLL5232B BY FULL POWER
ZD4	93L 39149	MLL5232B BY FULL POWER
ZD5	93L 39149	MLL5232B BY FULL POWER
ZD6	93L 39149	MLL5232B BY FULL POWER
D3	93L 60211	SMB340 BY FULL POWER SM
D4	93L 60211	SMB340 BY FULL POWER SM
D1	93L 60222	BAT54CFILM
D1	93L 60230	BAT54C
D2	93L 64 32	LL4148 SMD
D2	93L 6432V	LL4148-GS08-SMT
	715L 939 1	LCD 15" COMPAQ MAIN BRD

PARTS LIST OF KEY PC BOARD

LOCATION	**KEPC560KB1**	**SPECIFICATION**
SW1	77L 600 1GHJ	KEY SWITCH
SW2	77L 600 1GHJ	KEY SWITCH
SW3	77L 600 1GHJ	KEY SWITCH
SW4	77L 600 1GHJ	KEY SWITCH
D1	81L 12 1 BH	3 PIN LED
CN1	95L8014 7 2	HARNESS
	715L 934 1	LCD COMPAQ 17" KEY BRD

2.FP5017 FOR HANNSTAR*83 PANEL

PARTS LIST OF CABINET

LOCATION	TF1562-S3A	SPECIFICATION
	CBPC560KHDC2	CONVERSION BOARD FOR T56
	KEPC560KB3	KEY BOARD FOR T563K*COMP
	7L 1 L 3	WOODEN PALLET
	15L5689 2 A	GND CLAMP
	15L5753 1	MAIN BRACKET
	33L4438 A6 T	LOGO COVER
	40L 150716 5A	ID LABEL
	40L 152509	RECYCLE LABEL
	40L 152512	RECYCLE LABEL
	40L 154 14 1	CABINET LABEL
	40L 457716 1A	TCO99 LABEL
	40L 581 26704	軻繻 FOR CARTON/PALLET
	40L 581716 1A	CARTON LABEL
	40L 581716 4C	COLOREAL LABEL
	41L 68508 A	悢
	41L1500716 7B	DOC KIT(266987-A22)
	44L3231 15	EVA WASHER
	44L3231501	旧絫猧粗
	44L3231506	旧絫猧粗
	44L3510 1EPE	EPE-R
	44L3510 2EPE	EPE-L
	44L3510 5	U TYPE PAPER SHEET
	44L3510716 2B	CARTON
	44L9003 9	CORNER PAPER
	45L 77 3	ゴ 饯
	45L 77500	BARCODE RIBBON
	45L 77501	BARCODE RIBBON
	45L 88607 CP	PE BAG
	45L 88609	EPE COVER
	52L 1185 16	MIDDLE TAPE
	52L 1186	SMALL TAPE
	52L6020 2	PROTECT FILM
	52L6021 3	荡粲
	71L 100 19	WS ZP 5*12*25
	78L 311 1 L	SPEAKER 4 ohm 2W
	78L 311 1 R	SPEAKER 4 ohm 2W
	79L L15 12 E	INVERTER BY EMAX
	80L L15 11 LS	ADAPTOR BY LINE SHIN
	80L L15 11 LT	ADAPTER
	85L 601 1	SHIELD CASE
	89L 173 56 8	AUDIO CABLE 1800mm BLACK
	89L 173L15 28	SIGNAL CABLE

	89L 176 40 2	FFC CABLE 40P 50mm
	89L410A18N IS	POWER CORD WALL-OUT FOR
	M1L 330 4128	SCREW M3X4
	M1L 330 6128	SCREW
	M1L1030 12128	SCREW M3X12
	M1L1740 10 47	SCREW M4X10
	Q1L1030 8 47	SCREW 3mmX8
	Q1L1030 10128	SCREW
	705L563KB34001	LCD 催 ASS'Y
	750LLH50X83	HANNSTAR 15" S.I PANEL (

PARTS LIST OF BACK COVER ASS'Y

LOCATION	705L563KB34001	SPECIFICATION
	12L 387 2	RUBBER FOOT
	15L5752 1	BASE BRACKET
	15L5754 1	VESA BRACKET
	15L5755 1	STAND BRACKET
	33L4434 1	LENS
	33L4435 A5 L	KEY PAD
	33L4437 A7 L	POWER BUTTON
	33L4439 A6 L	HOOL COVER
	34L 969AA5 T	FRONT PANEL
	34L 970AA6 2T	BACK COVER
	34L 971 A6 B	PEDESTAL
	37L 456 1	HINGE
	M1L1740 8128	SCREW M4X8
	Q1L 340 10128	SCREW 4X10mm
	Q1L1040 8128	SCREW 4X8mm
	Q1L 140 8128	SCREW

PARTS LIST OF CONVERSION BOARD

LOCATION	CBPC560KHDC2	SPECIFICATION
	AI560KHDC2	CBPC AUTO INS.FOR T563K*
CN11	33L3802 2	WAFER EH-2
CN7	33L3802 2	WAFER EH-2
CN5	33L3802 7	WAFER EH-7
CN9	33L3802 4H	WAFER 4P RIGHT ANGLE
CN10	33L3802 5H	WAFER 5P RIGHT ANELE PIT
CN6	33L8022 6A H	HEADER FEMALE 6P
	40L 457624 1A	CPU LABEL
	40L 581624 2B	CHASSIS LABEL
	49L 51 1A	簕猳
	55L 100600 A	ň 盼瞜奎
	55L 100603	κ て瞜奎

U5	56L1133 35 H1	W49F 002UP
C101	67L 305331 4	330UF +-20% 25V
C79	67L 305331 4	330UF +-20% 25V
C95	67L 305331 4	330UF +-20% 25V
L5	71L 55 28	FERRITE BEAD 7.62*5.08*6
CN8	88L 302 4C	PHONE JACK
CN12	88L 304 8K	DC POWER JACK SCD-014A B
CN1	88L 35315F HS	D-SUB 15PIN FEMALE
X1	93L 22 53	CRYSTAL 14.318MHzHC-49US

PARTS LIST OF CONVERSION BOARD AUTO INSERTION

LOCATION	AI560KHDC2	SPECIFICATION
CN3	33L8019 40	CONNECTOR 40P SMT
CN4	33L8019 40	CONNECTOR 40P SMT
	55L 23500	猳海柴睦警
	55L 100600 A	ň 玢嘍奎
	55L 100602	奎籌
U3	56L 562 17	GM2115
U7	56L 585 4	AIC1117-33CY SMT
U9	56L 585 5	RT9164-25CG
U8	56L 621 2	LM4863MTEX
U10	56L 622 1	BA9741F-SMT
U6	56L1133 33	M24C16-MN6T SMT
U1	56L1133 34	M24C02-WMN6T SMT
U2	56L4LVC 14 F	74LVC14 BY FAIRCHILD
U2	56L4LVC 14 P	74LVC14ADT
Q2	57L 417 4	PMBS3904/PHILIPS-SMT
Q3	57L 417 4	PMBS3904/PHILIPS-SMT
Q6	57L 417 4	PMBS3904/PHILIPS-SMT
Q5	57L 417 6	PMBS3906/PHILIPS-SMT
Q8	57L 417 6	PMBS3906/PHILIPS-SMT
Q1	57L 763 1	A03401 SOT23 BY AO
Q4	57L 763 2	AO4403 SO-8 BY AOS SMT
Q7	57L 763 2	AO4403 SO-8 BY AOS SMT
RP4	61L 125103 8	CHIP AR 8P4R 10KOHM +-5%
RP6	61L 125472 8	CHIP AR 8P4R 4.7K OHM+-5
R57	61L0603100	CHIP 10 OHM 1/16W
R1	61L0603101	CHIPR 100 OHM +-5% 1/16W
R2	61L0603101	CHIPR 100 OHM +-5% 1/16W
R5	61L0603101	CHIPR 100 OHM +-5% 1/16W
R6	61L0603101	CHIPR 100 OHM +-5% 1/16W
R60	61L0603101	CHIPR 100 OHM +-5% 1/16W
R71	61L0603101	CHIPR 100 OHM +-5% 1/16W
R8	61L0603101	CHIPR 100 OHM +-5% 1/16W
R9	61L0603101	CHIPR 100 OHM +-5% 1/16W

R29	61L0603102	CHIPR 1K OHM +-5% 1/16W
R37	61L0603102	CHIPR 1K OHM +-5% 1/16W
R48	61L0603102	CHIPR 1K OHM +-5% 1/16W
R49	61L0603102	CHIPR 1K OHM +-5% 1/16W
R54	61L0603102	CHIPR 1K OHM +-5% 1/16W
R70	61L0603102	CHIPR 1K OHM +-5% 1/16W
R14	61L0603103	CHIPR 10K OHM +-5% 1/16W
R3	61L0603103	CHIPR 10K OHM +-5% 1/16W
R30	61L0603103	CHIPR 10K OHM +-5% 1/16W
R31	61L0603103	CHIPR 10K OHM +-5% 1/16W
R35	61L0603103	CHIPR 10K OHM +-5% 1/16W
R36	61L0603103	CHIPR 10K OHM +-5% 1/16W
R38	61L0603103	CHIPR 10K OHM +-5% 1/16W
R39	61L0603103	CHIPR 10K OHM +-5% 1/16W
R4	61L0603103	CHIPR 10K OHM +-5% 1/16W
R40	61L0603103	CHIPR 10K OHM +-5% 1/16W
R45	61L0603103	CHIPR 10K OHM +-5% 1/16W
R52	61L0603103	CHIPR 10K OHM +-5% 1/16W
R68	61L0603103	CHIPR 10K OHM +-5% 1/16W
R73	61L0603103	CHIPR 10K OHM +-5% 1/16W
R78	61L0603103	CHIPR 10K OHM +-5% 1/16W
R79	61L0603103	CHIPR 10K OHM +-5% 1/16W
R43	61L0603104	CHIPR 100K OHM +-5% 1/16
R74	61L0603104	CHIPR 100K OHM +-5% 1/16
R75	61L0603104	CHIPR 100K OHM +-5% 1/16
R65	61L0603123	CHIP 12K OHM 1/16W
R61	61L0603183	CHIP 18K OHM 1/16W
R69	61L0603183	CHIP 18K OHM 1/16W
R16	61L0603202	CHIPR 2K OHM+-5% 1/16W
R17	61L0603202	CHIPR 2K OHM+-5% 1/16W
R47	61L0603203	CHIPR 20K OHM+-5% 1/16W
R50	61L0603203	CHIPR 20K OHM+-5% 1/16W
R62	61L0603203	CHIPR 20K OHM+-5% 1/16W
R41	61L0603221	CHIPR 220 OHM+-5% 1/16W
R42	61L0603221	CHIPR 220 OHM+-5% 1/16W
R24	61L0603272	CHIP 2.7K OHM 1/16W
R76	61L0603301	CHIP 300 OHM 1/16W
R77	61L0603301	CHIP 300 OHM 1/16W
R58	61L0603303	CHIP 30K OHM 5% 1/16W
R63	61L0603303	CHIP 30K OHM 5% 1/16W
R72	61L0603303	CHIP 30K OHM 5% 1/16W
R46	61L0603393	39K OHM+-5%
R51	61L0603393	39K OHM+-5%
R10	61L0603470	CHIPR 47 OHM +-5% 1/16W
R18	61L0603470	CHIPR 47 OHM +-5% 1/16W
R19	61L0603470	CHIPR 47 OHM +-5% 1/16W
R7	61L0603470	CHIPR 47 OHM +-5% 1/16W
R15	61L0603472	CHIPR 4.7K OHM +-5% 1/16

R23	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R25	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R32	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R33	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R44	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R53	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R56	61L0603473	CHIP 47K OHM 1/16W
R59	61L0603473	CHIP 47K OHM 1/16W
R64	61L0603473	CHIP 47K OHM 1/16W
R67	61L0603473	CHIP 47K OHM 1/16W
R55	61L0603563	CHIP 56K OHM 1/16W
R66	61L0603563	CHIP 56K OHM 1/16W
R11	61L0603750 9F	75OHM 1%
R12	61L0603750 9F	75OHM 1%
R13	61L0603750 9F	75OHM 1%
CP1	65L 600220 8T	22PF+-10% 50V 8P NPO SMD
CP10	65L 600220 8T	22PF+-10% 50V 8P NPO SMD
CP2	65L 600220 8T	22PF+-10% 50V 8P NPO SMD
CP3	65L 600220 8T	22PF+-10% 50V 8P NPO SMD
CP4	65L 600220 8T	22PF+-10% 50V 8P NPO SMD
CP5	65L 600220 8T	22PF+-10% 50V 8P NPO SMD
CP6	65L 600220 8T	22PF+-10% 50V 8P NPO SMD
CP7	65L 600220 8T	22PF+-10% 50V 8P NPO SMD
CP8	65L 600220 8T	22PF+-10% 50V 8P NPO SMD
CP9	65L 600220 8T	22PF+-10% 50V 8P NPO SMD
C103	65L0603101 32	100PF +-10% 50V X7R
C104	65L0603101 32	100PF +-10% 50V X7R
C111	65L0603101 32	100PF +-10% 50V X7R
C112	65L0603101 32	100PF +-10% 50V X7R
C113	65L0603101 32	100PF +-10% 50V X7R
C114	65L0603101 32	100PF +-10% 50V X7R
C115	65L0603101 32	100PF +-10% 50V X7R
C116	65L0603101 32	100PF +-10% 50V X7R
C118	65L0603101 32	100PF +-10% 50V X7R
C119	65L0603101 32	100PF +-10% 50V X7R
C126	65L0603101 32	100PF +-10% 50V X7R
C127	65L0603101 32	100PF +-10% 50V X7R
C105	65L0603102 32	CHIP 1000PF 50V X7R
C106	65L0603102 32	CHIP 1000PF 50V X7R
C107	65L0603102 32	CHIP 1000PF 50V X7R
C108	65L0603102 32	CHIP 1000PF 50V X7R
C109	65L0603102 32	CHIP 1000PF 50V X7R
C110	65L0603102 32	CHIP 1000PF 50V X7R
C117	65L0603102 32	CHIP 1000PF 50V X7R
C121	65L0603102 32	CHIP 1000PF 50V X7R
C122	65L0603102 32	CHIP 1000PF 50V X7R
C125	65L0603102 32	CHIP 1000PF 50V X7R
C62	65L0603102 32	CHIP 1000PF 50V X7R

C75	65L0603102 32	CHIP 1000PF 50V X7R
C86	65L0603102 32	CHIP 1000PF 50V X7R
C90	65L0603102 32	CHIP 1000PF 50V X7R
C1	65L0603103 32	0.01UF+-10% 50V X7R
C2	65L0603103 32	0.01UF+-10% 50V X7R
C4	65L0603103 32	0.01UF+-10% 50V X7R
C5	65L0603103 32	0.01UF+-10% 50V X7R
C6	65L0603103 32	0.01UF+-10% 50V X7R
C7	65L0603103 32	0.01UF+-10% 50V X7R
C76	65L0603103 32	0.01UF+-10% 50V X7R
C85	65L0603103 32	0.01UF+-10% 50V X7R
C89	65L0603103 32	0.01UF+-10% 50V X7R
C10	65L0603104 12	0.1UF +-10% 16V X7R
C102	65L0603104 12	0.1UF +-10% 16V X7R
C13	65L0603104 12	0.1UF +-10% 16V X7R
C14	65L0603104 12	0.1UF +-10% 16V X7R
C15	65L0603104 12	0.1UF +-10% 16V X7R
C16	65L0603104 12	0.1UF +-10% 16V X7R
C18	65L0603104 12	0.1UF +-10% 16V X7R
C19	65L0603104 12	0.1UF +-10% 16V X7R
C20	65L0603104 12	0.1UF +-10% 16V X7R
C21	65L0603104 12	0.1UF +-10% 16V X7R
C22	65L0603104 12	0.1UF +-10% 16V X7R
C23	65L0603104 12	0.1UF +-10% 16V X7R
C24	65L0603104 12	0.1UF +-10% 16V X7R
C25	65L0603104 12	0.1UF +-10% 16V X7R
C26	65L0603104 12	0.1UF +-10% 16V X7R
C27	65L0603104 12	0.1UF +-10% 16V X7R
C28	65L0603104 12	0.1UF +-10% 16V X7R
C3	65L0603104 12	0.1UF +-10% 16V X7R
C32	65L0603104 12	0.1UF +-10% 16V X7R
C33	65L0603104 12	0.1UF +-10% 16V X7R
C34	65L0603104 12	0.1UF +-10% 16V X7R
C35	65L0603104 12	0.1UF +-10% 16V X7R
C36	65L0603104 12	0.1UF +-10% 16V X7R
C37	65L0603104 12	0.1UF +-10% 16V X7R
C38	65L0603104 12	0.1UF +-10% 16V X7R
C39	65L0603104 12	0.1UF +-10% 16V X7R
C40	65L0603104 12	0.1UF +-10% 16V X7R
C41	65L0603104 12	0.1UF +-10% 16V X7R
C42	65L0603104 12	0.1UF +-10% 16V X7R
C43	65L0603104 12	0.1UF +-10% 16V X7R
C44	65L0603104 12	0.1UF +-10% 16V X7R
C46	65L0603104 12	0.1UF +-10% 16V X7R
C47	65L0603104 12	0.1UF +-10% 16V X7R
C48	65L0603104 12	0.1UF +-10% 16V X7R
C49	65L0603104 12	0.1UF +-10% 16V X7R
C50	65L0603104 12	0.1UF +-10% 16V X7R

C52	65L0603104 12	0.1UF +-10% 16V X7R
C56	65L0603104 12	0.1UF +-10% 16V X7R
C57	65L0603104 12	0.1UF +-10% 16V X7R
C58	65L0603104 12	0.1UF +-10% 16V X7R
C60	65L0603104 12	0.1UF +-10% 16V X7R
C64	65L0603104 12	0.1UF +-10% 16V X7R
C67	65L0603104 12	0.1UF +-10% 16V X7R
C69	65L0603104 12	0.1UF +-10% 16V X7R
C77	65L0603104 12	0.1UF +-10% 16V X7R
C84	65L0603104 12	0.1UF +-10% 16V X7R
C88	65L0603104 12	0.1UF +-10% 16V X7R
C96	65L0603104 12	0.1UF +-10% 16V X7R
C97	65L0603104 12	0.1UF +-10% 16V X7R
C98	65L0603104 12	0.1UF +-10% 16V X7R
C70	65L0603105 17	1UF 16V Y5V
C73	65L0603105 17	1UF 16V Y5V
C92	65L0603105 17	1UF 16V Y5V
C93	65L0603105 17	1UF 16V Y5V
C94	65L0603105 17	1UF 16V Y5V
C128	65L0603220 31	CHIP 22PF 50V NPO
C129	65L0603220 31	CHIP 22PF 50V NPO
C130	65L0603220 31	CHIP 22PF 50V NPO
C131	65L0603220 31	CHIP 22PF 50V NPO
C132	65L0603220 31	CHIP 22PF 50V NPO
C133	65L0603220 31	CHIP 22PF 50V NPO
C72	65L0603334 17	CHIP 0.33UF 16V Y5V
C8	65L0603470 32	CHIP 47PF 50V X7R
C9	65L0603470 32	CHIP 47PF 50V X7R
C99	65L0603471 32	CHIP 470PF 50V X7R
C100	65L0603473 32	CHIP 0.047UF 50V X7R
C91	65L0603473 32	CHIP 0.047UF 50V X7R
C53	65L0603509 31	CHIP 5PF+-0.5PF 50V NPO
C55	65L0603509 31	CHIP 5PF+-0.5PF 50V NPO
CP1	65L602K220 8T	IRRAY CAP 22PF +-10% 16V
CP10	65L602K220 8T	IRRAY CAP 22PF +-10% 16V
CP2	65L602K220 8T	IRRAY CAP 22PF +-10% 16V
CP3	65L602K220 8T	IRRAY CAP 22PF +-10% 16V
CP4	65L602K220 8T	IRRAY CAP 22PF +-10% 16V
CP5	65L602K220 8T	IRRAY CAP 22PF +-10% 16V
CP6	65L602K220 8T	IRRAY CAP 22PF +-10% 16V
CP7	65L602K220 8T	IRRAY CAP 22PF +-10% 16V
CP8	65L602K220 8T	IRRAY CAP 22PF +-10% 16V
CP9	65L602K220 8T	IRRAY CAP 22PF +-10% 16V
C12	67L 312100 3	SMD 10uf +-20% 16V
C30	67L 312100 3	SMD 10uf +-20% 16V
C51	67L 312100 3	SMD 10uf +-20% 16V
C54	67L 312100 3	SMD 10uf +-20% 16V
C61	67L 312100 3	SMD 10uf +-20% 16V

C59	67L 312101 3	SMD 100UF +-20% 16V
C68	67L 312101 3	SMD 100UF +-20% 16V
C71	67L 312101 3	SMD 100UF +-20% 16V
C74	67L 312101 3	SMD 100UF +-20% 16V
C11	67L 312470 3	SMD EC 47UF 16V +-20%
C17	67L 312470 3	SMD EC 47UF 16V +-20%
C29	67L 312470 3	SMD EC 47UF 16V +-20%
C31	67L 312470 3	SMD EC 47UF 16V +-20%
C45	67L 312470 3	SMD EC 47UF 16V +-20%
C63	67L 312470 3	SMD EC 47UF 16V +-20%
C66	67L 312470 3	SMD EC 47UF 16V +-20%
C83	67L 312470 3	SMD EC 47UF 16V +-20%
C87	67L 312470 3	SMD EC 47UF 16V +-20%
RP1	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP10	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP11	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP12	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP2	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP3	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP5	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP7	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP8	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
RP9	71L 56A121 8T	CHIP BEAD ARRAY 120 OHM
FB1	71L 56Z601	CHIP BEAD 600 OHM 0805
FB2	71L 56Z601	CHIP BEAD 600 OHM 0805
FB3	71L 56Z601	CHIP BEAD 600 OHM 0805
FB4	71L 56Z601	CHIP BEAD 600 OHM 0805
FB5	71L 56Z601	CHIP BEAD 600 OHM 0805
FB6	71L 56Z601	CHIP BEAD 600 OHM 0805
R20	71L 59B121	TB160808B12 SMD
R21	71L 59B121	TB160808B12 SMD
R22	71L 59B121	TB160808B12 SMD
R26	71L 59B121	TB160808B12 SMD
R27	71L 59B121	TB160808B12 SMD
R28	71L 59B121	TB160808B12 SMD
R20	71L 59C121 B	FCM1608C-121T03 SMD
R21	71L 59C121 B	FCM1608C-121T03 SMD
R22	71L 59C121 B	FCM1608C-121T03 SMD
R26	71L 59C121 B	FCM1608C-121T03 SMD
R27	71L 59C121 B	FCM1608C-121T03 SMD
R28	71L 59C121 B	FCM1608C-121T03 SMD
L3	73L 253136 TE	CHOKE COIL BY TECSTAR
L4	73L 253136 TE	CHOKE COIL BY TECSTAR
U5	87L 202 32	PLCC CONN 32PIN
ZD1	93L 39146	LL5232B SMT
ZD2	93L 39146	LL5232B SMT
ZD3	93L 39146	LL5232B SMT
ZD4	93L 39146	LL5232B SMT

ZD5	93L 39146	LL5232B SMT
ZD6	93L 39146	LL5232B SMT
ZD1	93L 39147	TZMC5V6-GS08 SMT
ZD2	93L 39147	TZMC5V6-GS08 SMT
ZD3	93L 39147	TZMC5V6-GS08 SMT
ZD4	93L 39147	TZMC5V6-GS08 SMT
ZD5	93L 39147	TZMC5V6-GS08 SMT
ZD6	93L 39147	TZMC5V6-GS08 SMT
ZD1	93L 39149	MLL5232B BY FULL POWER S
ZD2	93L 39149	MLL5232B BY FULL POWER S
ZD3	93L 39149	MLL5232B BY FULL POWER S
ZD4	93L 39149	MLL5232B BY FULL POWER S
ZD5	93L 39149	MLL5232B BY FULL POWER S
ZD6	93L 39149	MLL5232B BY FULL POWER S
D3	93L 60211	SMB340 BY FULL POWER SMT
D4	93L 60211	SMB340 BY FULL POWER SMT
D1	93L 60222	BAT54CFILM
D1	93L 60230	BAT54C
D2	93L 64 32	LL4148 SMD
D2	93L 6432V	LL4148-GS08-SMT
	715L 939 1	LCD 15" COMPAQ MAIN BRD

PARTS LIST OF KEY PC BOARD

LOCATION	KEPC560KB3	SPECIFICATION
	AIK560KB3	KEY BOARD FOR T563K*CPQ
VR1	75L 35850322B	VR 50KB CRAY
SW1	77L 600 1GHJ	KEY SWITCH
SW2	77L 600 1GHJ	KEY SWITCH
SW3	77L 600 1GHJ	KEY SWITCH
SW4	77L 600 1GHJ	KEY SWITCH
D1	81L 12 1 BH	3 PIN LED
LN4	88L 302 4C	PHONE JACK
LN4	88L 302 4S	3.5MM EAR PHONE JACK
CN2	95L8014 4 2	HARNESS
CN3	95L8014 5 13	HARNESS
CN1	95L8014 7 2	HARNESS

PARTS LIST OF KEY PC BOARD AUTO INSERTION

LOCATION	AIK560KB3	SPECIFICATION
	715L 936 1	LCD 17" KEY BRD + SP
J1	95L 90 23	TIN COATED
J3	95L 90 23	TIN COATED
R1	61L 60233052T	CFR 33 OHM +-5% 1/6W
R2	61L 60233052T	CFR 33 OHM +-5% 1/6W

3.TFT5017 FOR CPT XG02 PANEL

PARTS LIST OF CABINET

LOCATION	TF1562-S3	SPECIFICATION
	CBPC560KCDC3	CONVERSION BOARD FOR T56
	KEPC560KB1	KEY BOARD FOR T563K*COMP
	15L5689 2 A	GND CLAMP
	15L5776 1	MAIN FRAME
	33L4438 A6 T	LOGO COVER
	40L 150716 1	ID LABEL
	40L 152509	RECYCLE LABEL
	40L 152512	RECYCLE LABEL
	40L 154 14 1	CABINET LABEL
	40L 457716 1A	TCO99 LABEL
	40L 581 26668	SLZ LABEL
	40L 581 26704	酮繷 FOR CARTON/PALLET
	40L 581689 4A	SERIAL LABEL FOR MONITOR
	40L 581716 4C	COLOREAL LABEL
	41L 68508 A	恨
	44L3231 15	EVA WASHER
	44L3510 1EPE	EPE-R
	44L3510 2EPE	EPE-L
	44L3510 5	U TYPE PAPER SHEET
	44L3510624 1A	CARTON
	45L 77 3	ゴ 饯
	45L 77500	BARCODE RIBBON
	45L 77501	BARCODE RIBBON
	45L 88607 CP	PE BAG
	45L 88609	EPE COVER
	52L 1185 16	MIDDLE TAPE
	52L 1186	SMALL TAPE
	52L6020 2	PROTECT FILM
	52L6021 3	荡粲
	71L 100 19	WS ZP 5*12*25
	79L L15 18 E	INVERTER BY EMAX
	80L L15 11 LS	ADAPTOR BY LINE SHIN
	80L L15 11 LT	ADAPTER
	85L 601 1	SHIELD CASE
	89L 173L15 28	SIGNAL CABLE
	89L 176 50 1	FPC CABLE 50P
	89L402A18N IS	POWER CORD
	95L8019 3 2	INVERTER LINE
	M1L 330 4128	SCREW M3X4
	M1L 330 6128	SCREW
	M1L1740 10 47	SCREW M4X10
	Q1L1030 8 47	SCREW 3mmX8

	Q1L1030 10128	SCREW
	750LLC50G02	CPT 15" LCD PANEL(G02)
	705L563KB34002	LCD 催 ASS'Y

PARTS LIST OF BACK COVER ASS'Y

LOCATION	705L563KB34002	SPECIFICATION
	12L 387 2	RUBBER FOOT
	15L5752 1	BASE BRACKET
	15L5754 1	VESA BRACKET
	15L5755 1	STAND BRACKET
	33L4434 1	LENS
	33L4435 A5 L	KEY PAD
	33L4436 A7 L	POWER BUTTON
	33L4439 A6 L	HOOL COVER
	34L 968AA5 T	FRONT PANEL
	34L 970AA6 1T	BACK COVER
	34L 971 A6 B	PEDESTAL
	37L 456 1	HINGE
	M1L1740 8128	SCREW M4X8
	Q1L 340 10128	SCREW 4X10mm
	Q1L 140 8128	SCREW

PARTS LIST OF CONVERSION BOARD

LOCATION	CBPC560KCDC3	SPECIFICATION
	AI560KCDC3	MAIN BOARD FOR T563K*CPQ
CN5	33L3802 7	WAFER EH-7
CN6	33L8022 6A H	HEADER FEMALE 6P
	33L8024 7	HEADER 7P FEMALE H=0 4mm
	40L 457624 1A	CPU LABEL
	40L 581624 2B	CHASSIS LABEL
	49L 51 1A	簕猳
	55L 100600 A	ň 盼瞜奎
	55L 100603	ĸ て瞜奎
U5	56L1133 35 C1	W49F 002UP
C101	67L 305331 4	330UF +-20% 25V
C79	67L 305331 4	330UF +-20% 25V
C95	67L 305331 4	330UF +-20% 25V
L5	71L 55 28	FERRITE BEAD 7.62*5.08*6
VR1	75L 335103	CFVR 10K OHM +-20%
U11	79LL15M 2CYN	DC/DC MODULE BY CYNTEC
CN12	88L 304 8K	DC POWER JACK SCD-014A B
CN1	88L 35315F HS	D-SUB 15PIN FEMALE
X1	93L 22 53	CRYSTAL 14.318MHzHC-49US

PARTS LIST OF CONVERSION BOARD AUTO INSERTION

LOCATION	AI560KCDC3	SPECIFICATION
CN3	33L3804 50	CONNECTOR 50P
CN4	33L3804 50	CONNECTOR 50P
	55L 23520	IPA
	55L 100600 A	ň 玢瞜奎
	55L 100602	奎篝
U3	56L 562 17	GM2115
U9	56L 585 5	RT9164-25CG
U10	56L 622 1	BA9741F-SMT
U6	56L1133 33	M24C16-MN6T SMT
U1	56L1133 34	M24C02-WMN6T SMT
U2	56L4LVC 14 F	74LVC14 BY FAIRCHILD
U2	56L4LVC 14 P	74LVC14ADT
Q2	57L 417 4	PMBS3904/PHILIPS-SMT
Q3	57L 417 4	PMBS3904/PHILIPS-SMT
Q6	57L 417 4	PMBS3904/PHILIPS-SMT
Q5	57L 417 6	PMBS3906/PHILIPS-SMT
Q8	57L 417 6	PMBS3906/PHILIPS-SMT
Q1	57L 763 1	A03401 SOT23 BY AO
Q4	57L 763 2	AO4403 SO-8 BY AOS SMT
Q7	57L 763 2	AO4403 SO-8 BY AOS SMT
RP4	61L 125103 8	CHIP AR 8P4R 10KOHM +-5%
LP1	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP10	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP11	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP12	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP13	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP2	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP3	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP4	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP5	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP6	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP7	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP8	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP9	61L 125330 8	CHIP AR 894R 33OHM +-5%
RP6	61L 125472 8	CHIP AR 8P4R 4.7K OHM+-5
R80	61L0603000	CHIPR 0OHM +-5% 1/16W
R82	61L0603000	CHIPR 0OHM +-5% 1/16W
R83	61L0603000	CHIPR 0OHM +-5% 1/16W
R57	61L0603100	CHIP 10 OHM 1/16W
R1	61L0603101	CHIPR 100 OHM +-5% 1/16W
R2	61L0603101	CHIPR 100 OHM +-5% 1/16W
R5	61L0603101	CHIPR 100 OHM +-5% 1/16W

R6	61L0603101	CHIPR 100 OHM +-5% 1/16W
R60	61L0603101	CHIPR 100 OHM +-5% 1/16W
R71	61L0603101	CHIPR 100 OHM +-5% 1/16W
R8	61L0603101	CHIPR 100 OHM +-5% 1/16W
R9	61L0603101	CHIPR 100 OHM +-5% 1/16W
R37	61L0603102	CHIPR 1K OHM +-5% 1/16W
R54	61L0603102	CHIPR 1K OHM +-5% 1/16W
R70	61L0603102	CHIPR 1K OHM +-5% 1/16W
R14	61L0603103	CHIPR 10K OHM +-5% 1/16W
R3	61L0603103	CHIPR 10K OHM +-5% 1/16W
R30	61L0603103	CHIPR 10K OHM +-5% 1/16W
R31	61L0603103	CHIPR 10K OHM +-5% 1/16W
R35	61L0603103	CHIPR 10K OHM +-5% 1/16W
R36	61L0603103	CHIPR 10K OHM +-5% 1/16W
R38	61L0603103	CHIPR 10K OHM +-5% 1/16W
R39	61L0603103	CHIPR 10K OHM +-5% 1/16W
R4	61L0603103	CHIPR 10K OHM +-5% 1/16W
R40	61L0603103	CHIPR 10K OHM +-5% 1/16W
R45	61L0603103	CHIPR 10K OHM +-5% 1/16W
R68	61L0603103	CHIPR 10K OHM +-5% 1/16W
R73	61L0603103	CHIPR 10K OHM +-5% 1/16W
R78	61L0603103	CHIPR 10K OHM +-5% 1/16W
R79	61L0603103	CHIPR 10K OHM +-5% 1/16W
R81	61L0603103	CHIPR 10K OHM +-5% 1/16W
R43	61L0603104	CHIPR 100K OHM +-5% 1/16
R85	61L0603104	CHIPR 100K OHM +-5% 1/16
R65	61L0603123	CHIP 12K OHM 1/16W
R61	61L0603183	CHIP 18K OHM 1/16W
R69	61L0603183	CHIP 18K OHM 1/16W
R16	61L0603202	CHIPR 2K OHM+-5% 1/16W
R17	61L0603202	CHIPR 2K OHM+-5% 1/16W
R62	61L0603203	CHIPR 20K OHM+-5% 1/16W
R41	61L0603221	CHIPR 220 OHM+-5% 1/16W
R42	61L0603221	CHIPR 220 OHM+-5% 1/16W
R24	61L0603272	CHIP 2.7K OHM 1/16W
R76	61L0603301	CHIP 300 OHM 1/16W
R77	61L0603301	CHIP 300 OHM 1/16W
R86	61L0603302	CHIPR 3K OHM +-5% 1/16W
R58	61L0603303	CHIP 30K OHM 5% 1/16W
R63	61L0603303	CHIP 30K OHM 5% 1/16W
R72	61L0603303	CHIP 30K OHM 5% 1/16W
R10	61L0603470	CHIPR 47 OHM +-5% 1/16W
R18	61L0603470	CHIPR 47 OHM +-5% 1/16W
R19	61L0603470	CHIPR 47 OHM +-5% 1/16W
R7	61L0603470	CHIPR 47 OHM +-5% 1/16W
R15	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R23	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R25	61L0603472	CHIPR 4.7K OHM +-5% 1/16

R32	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R33	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R44	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R56	61L0603473	CHIP 47K OHM 1/16W
R59	61L0603473	CHIP 47K OHM 1/16W
R64	61L0603473	CHIP 47K OHM 1/16W
R67	61L0603473	CHIP 47K OHM 1/16W
R55	61L0603563	CHIP 56K OHM 1/16W
R66	61L0603563	CHIP 56K OHM 1/16W
R11	61L0603750 9F	75OHM 1%
R12	61L0603750 9F	75OHM 1%
R13	61L0603750 9F	75OHM 1%
C105	65L0603102 32	CHIP 1000PF 50V X7R
C106	65L0603102 32	CHIP 1000PF 50V X7R
C107	65L0603102 32	CHIP 1000PF 50V X7R
C108	65L0603102 32	CHIP 1000PF 50V X7R
C109	65L0603102 32	CHIP 1000PF 50V X7R
C110	65L0603102 32	CHIP 1000PF 50V X7R
C117	65L0603102 32	CHIP 1000PF 50V X7R
C121	65L0603102 32	CHIP 1000PF 50V X7R
C122	65L0603102 32	CHIP 1000PF 50V X7R
C125	65L0603102 32	CHIP 1000PF 50V X7R
C139	65L0603102 32	CHIP 1000PF 50V X7R
C141	65L0603102 32	CHIP 1000PF 50V X7R
C144	65L0603102 32	CHIP 1000PF 50V X7R
C149	65L0603102 32	CHIP 1000PF 50V X7R
C150	65L0603102 32	CHIP 1000PF 50V X7R
C151	65L0603102 32	CHIP 1000PF 50V X7R
C152	65L0603102 32	CHIP 1000PF 50V X7R
C62	65L0603102 32	CHIP 1000PF 50V X7R
C75	65L0603102 32	CHIP 1000PF 50V X7R
C86	65L0603102 32	CHIP 1000PF 50V X7R
C90	65L0603102 32	CHIP 1000PF 50V X7R
C1	65L0603103 32	0.01UF+-10% 50V X7R
C2	65L0603103 32	0.01UF+-10% 50V X7R
C4	65L0603103 32	0.01UF+-10% 50V X7R
C5	65L0603103 32	0.01UF+-10% 50V X7R
C6	65L0603103 32	0.01UF+-10% 50V X7R
C7	65L0603103 32	0.01UF+-10% 50V X7R
C76	65L0603103 32	0.01UF+-10% 50V X7R
C85	65L0603103 32	0.01UF+-10% 50V X7R
C89	65L0603103 32	0.01UF+-10% 50V X7R
C10	65L0603104 32	CHIP 0.1UF 50V X7R
C102	65L0603104 32	CHIP 0.1UF 50V X7R
C13	65L0603104 32	CHIP 0.1UF 50V X7R
C135	65L0603104 32	CHIP 0.1UF 50V X7R
C14	65L0603104 32	CHIP 0.1UF 50V X7R
C140	65L0603104 32	CHIP 0.1UF 50V X7R

C143	65L0603104 32	CHIP 0.1UF 50V X7R
C146	65L0603104 32	CHIP 0.1UF 50V X7R
C15	65L0603104 32	CHIP 0.1UF 50V X7R
C16	65L0603104 32	CHIP 0.1UF 50V X7R
C18	65L0603104 32	CHIP 0.1UF 50V X7R
C19	65L0603104 32	CHIP 0.1UF 50V X7R
C20	65L0603104 32	CHIP 0.1UF 50V X7R
C21	65L0603104 32	CHIP 0.1UF 50V X7R
C22	65L0603104 32	CHIP 0.1UF 50V X7R
C23	65L0603104 32	CHIP 0.1UF 50V X7R
C24	65L0603104 32	CHIP 0.1UF 50V X7R
C25	65L0603104 32	CHIP 0.1UF 50V X7R
C26	65L0603104 32	CHIP 0.1UF 50V X7R
C27	65L0603104 32	CHIP 0.1UF 50V X7R
C28	65L0603104 32	CHIP 0.1UF 50V X7R
C3	65L0603104 32	CHIP 0.1UF 50V X7R
C32	65L0603104 32	CHIP 0.1UF 50V X7R
C33	65L0603104 32	CHIP 0.1UF 50V X7R
C34	65L0603104 32	CHIP 0.1UF 50V X7R
C35	65L0603104 32	CHIP 0.1UF 50V X7R
C36	65L0603104 32	CHIP 0.1UF 50V X7R
C37	65L0603104 32	CHIP 0.1UF 50V X7R
C38	65L0603104 32	CHIP 0.1UF 50V X7R
C39	65L0603104 32	CHIP 0.1UF 50V X7R
C40	65L0603104 32	CHIP 0.1UF 50V X7R
C41	65L0603104 32	CHIP 0.1UF 50V X7R
C42	65L0603104 32	CHIP 0.1UF 50V X7R
C43	65L0603104 32	CHIP 0.1UF 50V X7R
C44	65L0603104 32	CHIP 0.1UF 50V X7R
C56	65L0603104 32	CHIP 0.1UF 50V X7R
C57	65L0603104 32	CHIP 0.1UF 50V X7R
C58	65L0603104 32	CHIP 0.1UF 50V X7R
C60	65L0603104 32	CHIP 0.1UF 50V X7R
C64	65L0603104 32	CHIP 0.1UF 50V X7R
C67	65L0603104 32	CHIP 0.1UF 50V X7R
C77	65L0603104 32	CHIP 0.1UF 50V X7R
C84	65L0603104 32	CHIP 0.1UF 50V X7R
C88	65L0603104 32	CHIP 0.1UF 50V X7R
C96	65L0603104 32	CHIP 0.1UF 50V X7R
C97	65L0603104 32	CHIP 0.1UF 50V X7R
C98	65L0603104 32	CHIP 0.1UF 50V X7R
C92	65L0603105 17	1UF 16V Y5V
C93	65L0603105 17	1UF 16V Y5V
C94	65L0603105 17	1UF 16V Y5V
C129	65L0603220 31	CHIP 22PF 50V NPO
C130	65L0603220 31	CHIP 22PF 50V NPO
C131	65L0603220 31	CHIP 22PF 50V NPO
C132	65L0603220 31	CHIP 22PF 50V NPO

C8	65L0603470 32	CHIP 47PF 50V X7R
C9	65L0603470 32	CHIP 47PF 50V X7R
C99	65L0603471 32	CHIP 470PF 50V X7R
C100	65L0603473 32	CHIP 0.047UF 50V X7R
C91	65L0603473 32	CHIP 0.047UF 50V X7R
C53	65L0603509 31	CHIP 5PF+-0.5PF 50V NPO
C55	65L0603509 31	CHIP 5PF+-0.5PF 50V NPO
C134	65L0805105 37	CHIP 1UF 50V Y5V
C138	65L0805105 37	CHIP 1UF 50V Y5V
C147	65L0805105 37	CHIP 1UF 50V Y5V
C12	67L 312100 3	SMD 10uf +-20% 16V
C153	67L 312100 3	SMD 10uf +-20% 16V
C154	67L 312100 3	SMD 10uf +-20% 16V
C54	67L 312100 3	SMD 10uf +-20% 16V
C61	67L 312100 3	SMD 10uf +-20% 16V
C136	67L 312101 3	SMD 100UF +-20% 16V
C137	67L 312101 3	SMD 100UF +-20% 16V
C59	67L 312101 3	SMD 100UF +-20% 16V
C11	67L 312470 3	SMD EC 47UF 16V +-20%
C133	67L 312470 3	SMD EC 47UF 16V +-20%
C17	67L 312470 3	SMD EC 47UF 16V +-20%
C29	67L 312470 3	SMD EC 47UF 16V +-20%
C30	67L 312470 3	SMD EC 47UF 16V +-20%
C31	67L 312470 3	SMD EC 47UF 16V +-20%
C83	67L 312470 3	SMD EC 47UF 16V +-20%
C87	67L 312470 3	SMD EC 47UF 16V +-20%
C142	67L 312479 6	SMD EC 4.7UF+-20% 35V
C145	67L 312479 6	SMD EC 4.7UF+-20% 35V
C148	67L 312479 6	SMD EC 4.7UF+-20% 35V
FB1	71L 56Z601	CHIP BEAD 600 OHM 0805
FB2	71L 56Z601	CHIP BEAD 600 OHM 0805
FB3	71L 56Z601	CHIP BEAD 600 OHM 0805
FB4	71L 56Z601	CHIP BEAD 600 OHM 0805
R20	71L 59B121	TB160808B12 SMD
R22	71L 59B121	TB160808B12 SMD
R26	71L 59B121	TB160808B12 SMD
R27	71L 59B121	TB160808B12 SMD
R84	71L 59B121	TB160808B12 SMD
R20	71L 59C121 B	FCM1608C-121T03 SMD
R22	71L 59C121 B	FCM1608C-121T03 SMD
R26	71L 59C121 B	FCM1608C-121T03 SMD
R27	71L 59C121 B	FCM1608C-121T03 SMD
R84	71L 59C121 B	FCM1608C-121T03 SMD
L3	73L 253136 TE	CHOKE COIL BY TECSTAR
L4	73L 253136 TE	CHOKE COIL BY TECSTAR
U5	87L 202 32	PLCC CONN 32PIN
ZD1	93L 39146	LL5232B SMT
ZD2	93L 39146	LL5232B SMT

ZD3	93L 39146	LL5232B SMT
ZD4	93L 39146	LL5232B SMT
ZD5	93L 39146	LL5232B SMT
ZD6	93L 39146	LL5232B SMT
ZD1	93L 39147	TZMC5V6-GS08 SMT
ZD2	93L 39147	TZMC5V6-GS08 SMT
ZD3	93L 39147	TZMC5V6-GS08 SMT
ZD4	93L 39147	TZMC5V6-GS08 SMT
ZD5	93L 39147	TZMC5V6-GS08 SMT
ZD6	93L 39147	TZMC5V6-GS08 SMT
ZD1	93L 39149	MLL5232B BY FULL POWER S
ZD2	93L 39149	MLL5232B BY FULL POWER S
ZD3	93L 39149	MLL5232B BY FULL POWER S
ZD4	93L 39149	MLL5232B BY FULL POWER S
ZD5	93L 39149	MLL5232B BY FULL POWER S
ZD6	93L 39149	MLL5232B BY FULL POWER S
D3	93L 60211	SMB340 BY FULL POWER SMT
D4	93L 60211	SMB340 BY FULL POWER SMT
D1	93L 60222	BAT54CFILM
D1	93L 60230	BAT54C
D2	93L 64 32	LL4148 SMD
D2	93L 6432V	LL4148-GS08-SMT
	715L 980 1	LCD 15"COMPAQ MAIN BOARD

PARTS LIST OF KEY PC BOARD

LOCATION	KEPC560KB1	SPECIFICATION
SW1	77L 600 1GHJ	KEY SWITCH
SW2	77L 600 1GHJ	KEY SWITCH
SW3	77L 600 1GHJ	KEY SWITCH
SW4	77L 600 1GHJ	KEY SWITCH
D1	81L 12 1 BH	3 PIN LED
CN1	95L8014 7 2	HARNESS
	715L 934 1	LCD COMPAQ 17" KEY BRD

4.FP5017 FOR CPT XG02 PANEL

PARTS LIST OF CABINET

LOCATION	TF1562-S3A	SPECIFICATION
	CBPC560KCDC2	CONVERSION BOARD FOR T56
	KEPC560KB3	KEY BOARD FOR T563K*COMP
	15L5689 2 A	GND CLAMP
	15L5776 1	MAIN FRAME
	33L4438 A6 T	LOGO COVER

40L 150716 1	ID LABEL
40L 152509	RECYCLE LABEL
40L 152512	RECYCLE LABEL
40L 154 14 1	CABINET LABEL
40L 457716 1A	TCO99 LABEL
40L 581 26668	SLZ LABEL
40L 581 26704	酮纀 FOR CARTON/PALLET
40L 581689 4A	SERIAL LABEL FOR MONITOR
40L 581716 4C	COLOREAL LABEL
41L 68508 A	恨
44L3231 15	EVA WASHER
44L3510 1EPE	EPE-R
44L3510 2EPE	EPE-L
44L3510 5	U TYPE PAPER SHEET
44L3510624 1A	CARTON
45L 77 3	ゴ 饯
45L 77500	BARCODE RIBBON
45L 77501	BARCODE RIBBON
45L 88607 CP	PE BAG
45L 88609	EPE COVER
52L 1185 16	MIDDLE TAPE
52L 1186	SMALL TAPE
52L6020 2	PROTECT FILM
52L6021 3	荡粲
71L 100 19	WS ZP 5*12*25
78L 311 1 L	SPEAKER 4 ohm 2W
78L 311 1 R	SPEAKER 4 ohm 2W
79L L15 18 E	INVERTER BY EMAX
80L L15 11 LS	ADAPTOR BY LINE SHIN
80L L15 11 LT	ADAPTER
85L 601 1	SHIELD CASE
89L 173 56 8	AUDIO CABLE 1800mm BLACK
89L 173L15 28	SIGNAL CABLE
89L 176 50 1	FPC CABLE 50P
89L402A18N IS	POWER CORD
95L8019 3 2	INVERTER LINE
M1L 330 4128	SCREW M3X4
M1L 330 6128	SCREW
M1L1740 10 47	SCREW M4X10
Q1L1030 8 47	SCREW 3mmX8
Q1L1030 10128	SCREW
750LLC50G02	CPT 15" LCD PANEL(G02)
705L563KB34001	LCD 催 ASS'Y

PARTS LIST OF BACK COVER ASS'Y

LOCATION	**705L563KB34001**	**SPECIFICATION**

12L 387 2	RUBBER FOOT
15L5752 1	BASE BRACKET
15L5754 1	VESA BRACKET
15L5755 1	STAND BRACKET
33L4434 1	LENS
33L4435 A5 L	KEY PAD
33L4437 A7 L	POWER BUTTON
33L4439 A6 L	HOOL COVER
34L 969AA5 T	FRONT PANEL
34L 970AA6 2T	BACK COVER
34L 971 A6 B	PEDESTAL
37L 456 1	HINGE
M1L1740 8128	SCREW M4X8
Q1L 340 10128	SCREW 4X10mm
Q1L1040 8128	SCREW 4X8mm
Q1L 140 8128	SCREW

PARTS LIST OF CONVERSION BOARD

LOCATION	CBPC560KCDC2	SPECIFICATION
	AI560KCDC2	MAIN BOARD FOR T563K*CPQ
CN11	33L3802 2	WAFER EH-2
CN7	33L3802 2	WAFER EH-2
CN5	33L3802 7	WAFER EH-7
CN9	33L3802 4H	WAFER 4P RIGHT ANGLE
CN10	33L3802 5H	WAFER 5P RIGHT ANELE PIT
CN6	33L8022 6A H	HEADER FEMALE 6P
	33L8024 7	HEADER 7P FEMALE H=0 4mm
	40L 457624 1A	CPU LABEL
	40L 581624 2B	CHASSIS LABEL
	49L 51 1A	簕猳
	55L 100600 A	ň 盼瞜奎
	55L 100603	κ て瞜奎
U5	56L1133 35 C1	W49F 002UP
C101	67L 305331 4	330UF +-20% 25V
C79	67L 305331 4	330UF +-20% 25V
C95	67L 305331 4	330UF +-20% 25V
L5	71L 55 28	FERRITE BEAD 7.62*5.08*6
VR1	75L 335103	CFVR 10K OHM +-20%
U11	79LL15M 2CYN	DC/DC MODULE BY CYNTEC
CN8	88L 302 4C	PHONE JACK
CN12	88L 304 8K	DC POWER JACK SCD-014A B
CN1	88L 35315F HS	D-SUB 15PIN FEMALE
X1	93L 22 53	CRYSTAL 14.318MHzHC-49US

PARTS LIST OF CONVERSION BOARD AUTO INSERTION

LOCATION	AI560KCDC2	SPECIFICATION
CN3	33L3804 50	CONNECTOR 50P
CN4	33L3804 50	CONNECTOR 50P
	55L 23500	猳海柴睦警
	55L 100600 A	ň 盼瞜奎
	55L 100602	奎籌
U3	56L 562 17	GM2115
U9	56L 585 5	RT9164-25CG
U8	56L 621 2	LM4863MTEX
U10	56L 622 1	BA9741F-SMT
U6	56L1133 33	M24C16-MN6T SMT
U1	56L1133 34	M24C02-WMN6T SMT
U2	56L4LVC 14 F	74LVC14 BY FAIRCHILD
U2	56L4LVC 14 P	74LVC14ADT
Q2	57L 417 4	PMBS3904/PHILIPS-SMT
Q3	57L 417 4	PMBS3904/PHILIPS-SMT
Q6	57L 417 4	PMBS3904/PHILIPS-SMT
Q5	57L 417 6	PMBS3906/PHILIPS-SMT
Q8	57L 417 6	PMBS3906/PHILIPS-SMT
Q1	57L 763 1	A03401 SOT23 BY AO
Q4	57L 763 2	AO4403 SO-8 BY AOS SMT
Q7	57L 763 2	AO4403 SO-8 BY AOS SMT
RP4	61L 125103 8	CHIP AR 8P4R 10KOHM +-5%
LP1	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP10	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP11	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP12	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP13	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP2	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP3	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP4	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP5	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP6	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP7	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP8	61L 125330 8	CHIP AR 894R 33OHM +-5%
LP9	61L 125330 8	CHIP AR 894R 33OHM +-5%
RP6	61L 125472 8	CHIP AR 8P4R 4.7K OHM+-5
R80	61L0603000	CHIPR 0OHM +-5% 1/16W
R82	61L0603000	CHIPR 0OHM +-5% 1/16W
R83	61L0603000	CHIPR 0OHM +-5% 1/16W
R57	61L0603100	CHIP 10 OHM 1/16W
R1	61L0603101	CHIPR 100 OHM +-5% 1/16W
R2	61L0603101	CHIPR 100 OHM +-5% 1/16W
R5	61L0603101	CHIPR 100 OHM +-5% 1/16W
R6	61L0603101	CHIPR 100 OHM +-5% 1/16W

R60	61L0603101	CHIPR 100 OHM +-5% 1/16W
R71	61L0603101	CHIPR 100 OHM +-5% 1/16W
R8	61L0603101	CHIPR 100 OHM +-5% 1/16W
R9	61L0603101	CHIPR 100 OHM +-5% 1/16W
R37	61L0603102	CHIPR 1K OHM +-5% 1/16W
R48	61L0603102	CHIPR 1K OHM +-5% 1/16W
R49	61L0603102	CHIPR 1K OHM +-5% 1/16W
R54	61L0603102	CHIPR 1K OHM +-5% 1/16W
R70	61L0603102	CHIPR 1K OHM +-5% 1/16W
R14	61L0603103	CHIPR 10K OHM +-5% 1/16W
R3	61L0603103	CHIPR 10K OHM +-5% 1/16W
R30	61L0603103	CHIPR 10K OHM +-5% 1/16W
R31	61L0603103	CHIPR 10K OHM +-5% 1/16W
R35	61L0603103	CHIPR 10K OHM +-5% 1/16W
R36	61L0603103	CHIPR 10K OHM +-5% 1/16W
R38	61L0603103	CHIPR 10K OHM +-5% 1/16W
R39	61L0603103	CHIPR 10K OHM +-5% 1/16W
R4	61L0603103	CHIPR 10K OHM +-5% 1/16W
R40	61L0603103	CHIPR 10K OHM +-5% 1/16W
R45	61L0603103	CHIPR 10K OHM +-5% 1/16W
R52	61L0603103	CHIPR 10K OHM +-5% 1/16W
R68	61L0603103	CHIPR 10K OHM +-5% 1/16W
R73	61L0603103	CHIPR 10K OHM +-5% 1/16W
R78	61L0603103	CHIPR 10K OHM +-5% 1/16W
R79	61L0603103	CHIPR 10K OHM +-5% 1/16W
R81	61L0603103	CHIPR 10K OHM +-5% 1/16W
R43	61L0603104	CHIPR 100K OHM +-5% 1/16
R74	61L0603104	CHIPR 100K OHM +-5% 1/16
R75	61L0603104	CHIPR 100K OHM +-5% 1/16
R85	61L0603104	CHIPR 100K OHM +-5% 1/16
R65	61L0603123	CHIP 12K OHM 1/16W
R61	61L0603183	CHIP 18K OHM 1/16W
R69	61L0603183	CHIP 18K OHM 1/16W
R16	61L0603202	CHIPR 2K OHM+-5% 1/16W
R17	61L0603202	CHIPR 2K OHM+-5% 1/16W
R47	61L0603203	CHIPR 20K OHM+-5% 1/16W
R50	61L0603203	CHIPR 20K OHM+-5% 1/16W
R62	61L0603203	CHIPR 20K OHM+-5% 1/16W
R41	61L0603221	CHIPR 220 OHM+-5% 1/16W
R42	61L0603221	CHIPR 220 OHM+-5% 1/16W
R24	61L0603272	CHIP 2.7K OHM 1/16W
R76	61L0603301	CHIP 300 OHM 1/16W
R77	61L0603301	CHIP 300 OHM 1/16W
R86	61L0603302	CHIPR 3K OHM +-5% 1/16W
R58	61L0603303	CHIP 30K OHM 5% 1/16W
R63	61L0603303	CHIP 30K OHM 5% 1/16W
R72	61L0603303	CHIP 30K OHM 5% 1/16W
R46	61L0603393	39K OHM+-5%

R51	61L0603393	39K OHM+-5%
R10	61L0603470	CHIPR 47 OHM +-5% 1/16W
R18	61L0603470	CHIPR 47 OHM +-5% 1/16W
R19	61L0603470	CHIPR 47 OHM +-5% 1/16W
R7	61L0603470	CHIPR 47 OHM +-5% 1/16W
R15	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R23	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R25	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R32	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R33	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R44	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R53	61L0603472	CHIPR 4.7K OHM +-5% 1/16
R56	61L0603473	CHIP 47K OHM 1/16W
R59	61L0603473	CHIP 47K OHM 1/16W
R64	61L0603473	CHIP 47K OHM 1/16W
R67	61L0603473	CHIP 47K OHM 1/16W
R55	61L0603563	CHIP 56K OHM 1/16W
R66	61L0603563	CHIP 56K OHM 1/16W
R11	61L0603750 9F	75OHM 1%
R12	61L0603750 9F	75OHM 1%
R13	61L0603750 9F	75OHM 1%
C103	65L0603101 32	100PF +-10% 50V X7R
C104	65L0603101 32	100PF +-10% 50V X7R
C111	65L0603101 32	100PF +-10% 50V X7R
C112	65L0603101 32	100PF +-10% 50V X7R
C113	65L0603101 32	100PF +-10% 50V X7R
C114	65L0603101 32	100PF +-10% 50V X7R
C115	65L0603101 32	100PF +-10% 50V X7R
C116	65L0603101 32	100PF +-10% 50V X7R
C118	65L0603101 32	100PF +-10% 50V X7R
C119	65L0603101 32	100PF +-10% 50V X7R
C126	65L0603101 32	100PF +-10% 50V X7R
C127	65L0603101 32	100PF +-10% 50V X7R
C105	65L0603102 32	CHIP 1000PF 50V X7R
C106	65L0603102 32	CHIP 1000PF 50V X7R
C107	65L0603102 32	CHIP 1000PF 50V X7R
C108	65L0603102 32	CHIP 1000PF 50V X7R
C109	65L0603102 32	CHIP 1000PF 50V X7R
C110	65L0603102 32	CHIP 1000PF 50V X7R
C117	65L0603102 32	CHIP 1000PF 50V X7R
C121	65L0603102 32	CHIP 1000PF 50V X7R
C122	65L0603102 32	CHIP 1000PF 50V X7R
C125	65L0603102 32	CHIP 1000PF 50V X7R
C135	65L0603104 32	CHIP 0.1UF 50V X7R
C14	65L0603104 32	CHIP 0.1UF 50V X7R
C140	65L0603104 32	CHIP 0.1UF 50V X7R
C143	65L0603104 32	CHIP 0.1UF 50V X7R
C146	65L0603104 32	CHIP 0.1UF 50V X7R

C15	65L0603104 32	CHIP 0.1UF 50V X7R
C16	65L0603104 32	CHIP 0.1UF 50V X7R
C18	65L0603104 32	CHIP 0.1UF 50V X7R
C19	65L0603104 32	CHIP 0.1UF 50V X7R
C20	65L0603104 32	CHIP 0.1UF 50V X7R
C21	65L0603104 32	CHIP 0.1UF 50V X7R
C22	65L0603104 32	CHIP 0.1UF 50V X7R
C23	65L0603104 32	CHIP 0.1UF 50V X7R
C24	65L0603104 32	CHIP 0.1UF 50V X7R
C25	65L0603104 32	CHIP 0.1UF 50V X7R
C26	65L0603104 32	CHIP 0.1UF 50V X7R
C27	65L0603104 32	CHIP 0.1UF 50V X7R
C28	65L0603104 32	CHIP 0.1UF 50V X7R
C3	65L0603104 32	CHIP 0.1UF 50V X7R
C32	65L0603104 32	CHIP 0.1UF 50V X7R
C33	65L0603104 32	CHIP 0.1UF 50V X7R
C34	65L0603104 32	CHIP 0.1UF 50V X7R
C35	65L0603104 32	CHIP 0.1UF 50V X7R
C36	65L0603104 32	CHIP 0.1UF 50V X7R
C37	65L0603104 32	CHIP 0.1UF 50V X7R
C38	65L0603104 32	CHIP 0.1UF 50V X7R
C39	65L0603104 32	CHIP 0.1UF 50V X7R
C40	65L0603104 32	CHIP 0.1UF 50V X7R
C41	65L0603104 32	CHIP 0.1UF 50V X7R
C42	65L0603104 32	CHIP 0.1UF 50V X7R
C43	65L0603104 32	CHIP 0.1UF 50V X7R
C44	65L0603104 32	CHIP 0.1UF 50V X7R
C56	65L0603104 32	CHIP 0.1UF 50V X7R
C57	65L0603104 32	CHIP 0.1UF 50V X7R
C58	65L0603104 32	CHIP 0.1UF 50V X7R
C60	65L0603104 32	CHIP 0.1UF 50V X7R
C64	65L0603104 32	CHIP 0.1UF 50V X7R
C67	65L0603104 32	CHIP 0.1UF 50V X7R
C69	65L0603104 32	CHIP 0.1UF 50V X7R
C77	65L0603104 32	CHIP 0.1UF 50V X7R
C84	65L0603104 32	CHIP 0.1UF 50V X7R
C88	65L0603104 32	CHIP 0.1UF 50V X7R
C96	65L0603104 32	CHIP 0.1UF 50V X7R
C97	65L0603104 32	CHIP 0.1UF 50V X7R
C98	65L0603104 32	CHIP 0.1UF 50V X7R
C70	65L0603105 17	1UF 16V Y5V
C73	65L0603105 17	1UF 16V Y5V
C92	65L0603105 17	1UF 16V Y5V
C93	65L0603105 17	1UF 16V Y5V
C94	65L0603105 17	1UF 16V Y5V
C129	65L0603220 31	CHIP 22PF 50V NPO
C130	65L0603220 31	CHIP 22PF 50V NPO
C131	65L0603220 31	CHIP 22PF 50V NPO

C132	65L0603220 31	CHIP 22PF 50V NPO
C72	65L0603334 17	CHIP 0.33UF 16V Y5V
C8	65L0603470 32	CHIP 47PF 50V X7R
C9	65L0603470 32	CHIP 47PF 50V X7R
C99	65L0603471 32	CHIP 470PF 50V X7R
C100	65L0603473 32	CHIP 0.047UF 50V X7R
C91	65L0603473 32	CHIP 0.047UF 50V X7R
C53	65L0603509 31	CHIP 5PF+-0.5PF 50V NPO
C55	65L0603509 31	CHIP 5PF+-0.5PF 50V NPO
C134	65L0805105 37	CHIP 1UF 50V Y5V
C138	65L0805105 37	CHIP 1UF 50V Y5V
C147	65L0805105 37	CHIP 1UF 50V Y5V
C12	67L 312100 3	SMD 10uf +-20% 16V
C153	67L 312100 3	SMD 10uf +-20% 16V
C154	67L 312100 3	SMD 10uf +-20% 16V
C54	67L 312100 3	SMD 10uf +-20% 16V
C61	67L 312100 3	SMD 10uf +-20% 16V
C136	67L 312101 3	SMD 100UF +-20% 16V
C137	67L 312101 3	SMD 100UF +-20% 16V
C59	67L 312101 3	SMD 100UF +-20% 16V
C68	67L 312101 3	SMD 100UF +-20% 16V
C71	67L 312101 3	SMD 100UF +-20% 16V
C74	67L 312101 3	SMD 100UF +-20% 16V
C11	67L 312470 3	SMD EC 47UF 16V +-20%
C133	67L 312470 3	SMD EC 47UF 16V +-20%
C17	67L 312470 3	SMD EC 47UF 16V +-20%
C29	67L 312470 3	SMD EC 47UF 16V +-20%
C30	67L 312470 3	SMD EC 47UF 16V +-20%
C31	67L 312470 3	SMD EC 47UF 16V +-20%
C83	67L 312470 3	SMD EC 47UF 16V +-20%
C87	67L 312470 3	SMD EC 47UF 16V +-20%
C142	67L 312479 6	SMD EC 4.7UF+-20% 35V
C145	67L 312479 6	SMD EC 4.7UF+-20% 35V
C148	67L 312479 6	SMD EC 4.7UF+-20% 35V
FB1	71L 56Z601	CHIP BEAD 600 OHM 0805
FB2	71L 56Z601	CHIP BEAD 600 OHM 0805
FB3	71L 56Z601	CHIP BEAD 600 OHM 0805
FB4	71L 56Z601	CHIP BEAD 600 OHM 0805
R20	71L 59B121	TB160808B12 SMD
R22	71L 59B121	TB160808B12 SMD
R26	71L 59B121	TB160808B12 SMD
R27	71L 59B121	TB160808B12 SMD
R84	71L 59B121	TB160808B12 SMD
R20	71L 59C121 B	FCM1608C-121T03 SMD
R22	71L 59C121 B	FCM1608C-121T03 SMD
R26	71L 59C121 B	FCM1608C-121T03 SMD
R27	71L 59C121 B	FCM1608C-121T03 SMD
R84	71L 59C121 B	FCM1608C-121T03 SMD

L3	73L 253136 TE	CHOKE COIL BY TECSTAR
L4	73L 253136 TE	CHOKE COIL BY TECSTAR
U5	87L 202 32	PLCC CONN 32PIN
ZD1	93L 39146	LL5232B SMT
ZD2	93L 39146	LL5232B SMT
ZD3	93L 39146	LL5232B SMT
ZD4	93L 39146	LL5232B SMT
ZD5	93L 39146	LL5232B SMT
ZD6	93L 39146	LL5232B SMT
ZD1	93L 39147	TZMC5V6-GS08 SMT
ZD2	93L 39147	TZMC5V6-GS08 SMT
ZD3	93L 39147	TZMC5V6-GS08 SMT
C87	67L 312470 3	SMD EC 47UF 16V +-20%
C142	67L 312479 6	SMD EC 4.7UF+-20% 35V
C145	67L 312479 6	SMD EC 4.7UF+-20% 35V
C148	67L 312479 6	SMD EC 4.7UF+-20% 35V
FB1	71L 56Z601	CHIP BEAD 600 OHM 0805
FB2	71L 56Z601	CHIP BEAD 600 OHM 0805
FB3	71L 56Z601	CHIP BEAD 600 OHM 0805
FB4	71L 56Z601	CHIP BEAD 600 OHM 0805
R20	71L 59B121	TB160808B12 SMD
R22	71L 59B121	TB160808B12 SMD
R26	71L 59C121 B	FCM1608C-121T03 SMD
R27	71L 59C121 B	FCM1608C-121T03 SMD
R84	71L 59C121 B	FCM1608C-121T03 SMD
L3	73L 253136 TE	CHOKE COIL BY TECSTAR
L4	73L 253136 TE	CHOKE COIL BY TECSTAR
U5	87L 202 32	PLCC CONN 32PIN
ZD1	93L 39146	LL5232B SMT
ZD2	93L 39146	LL5232B SMT
ZD3	93L 39146	LL5232B SMT
ZD4	93L 39146	LL5232B SMT
ZD5	93L 39146	LL5232B SMT
ZD6	93L 39146	LL5232B SMT
ZD1	93L 39147	TZMC5V6-GS08 SMT
ZD2	93L 39147	TZMC5V6-GS08 SMT
ZD3	93L 39147	TZMC5V6-GS08 SMT
ZD4	93L 39147	TZMC5V6-GS08 SMT
ZD5	93L 39147	TZMC5V6-GS08 SMT
ZD6	93L 39147	TZMC5V6-GS08 SMT
ZD1	93L 39149	MLL5232B BY FULL POWER S
ZD2	93L 39149	MLL5232B BY FULL POWER S
ZD3	93L 39149	MLL5232B BY FULL POWER S
ZD4	93L 39149	MLL5232B BY FULL POWER S
ZD5	93L 39149	MLL5232B BY FULL POWER S
ZD6	93L 39149	MLL5232B BY FULL POWER S
D3	93L 60211	SMB340 BY FULL POWER SMT
D4	93L 60211	SMB340 BY FULL POWER SMT

D1	93L 60222	BAT54CFILM
D1	93L 60230	BAT54C
D2	93L 64 32	LL4148 SMD
D2	93L 6432V	LL4148-GS08-SMT
	715L 980 1	LCD 15"COMPAQ MAIN BOARD

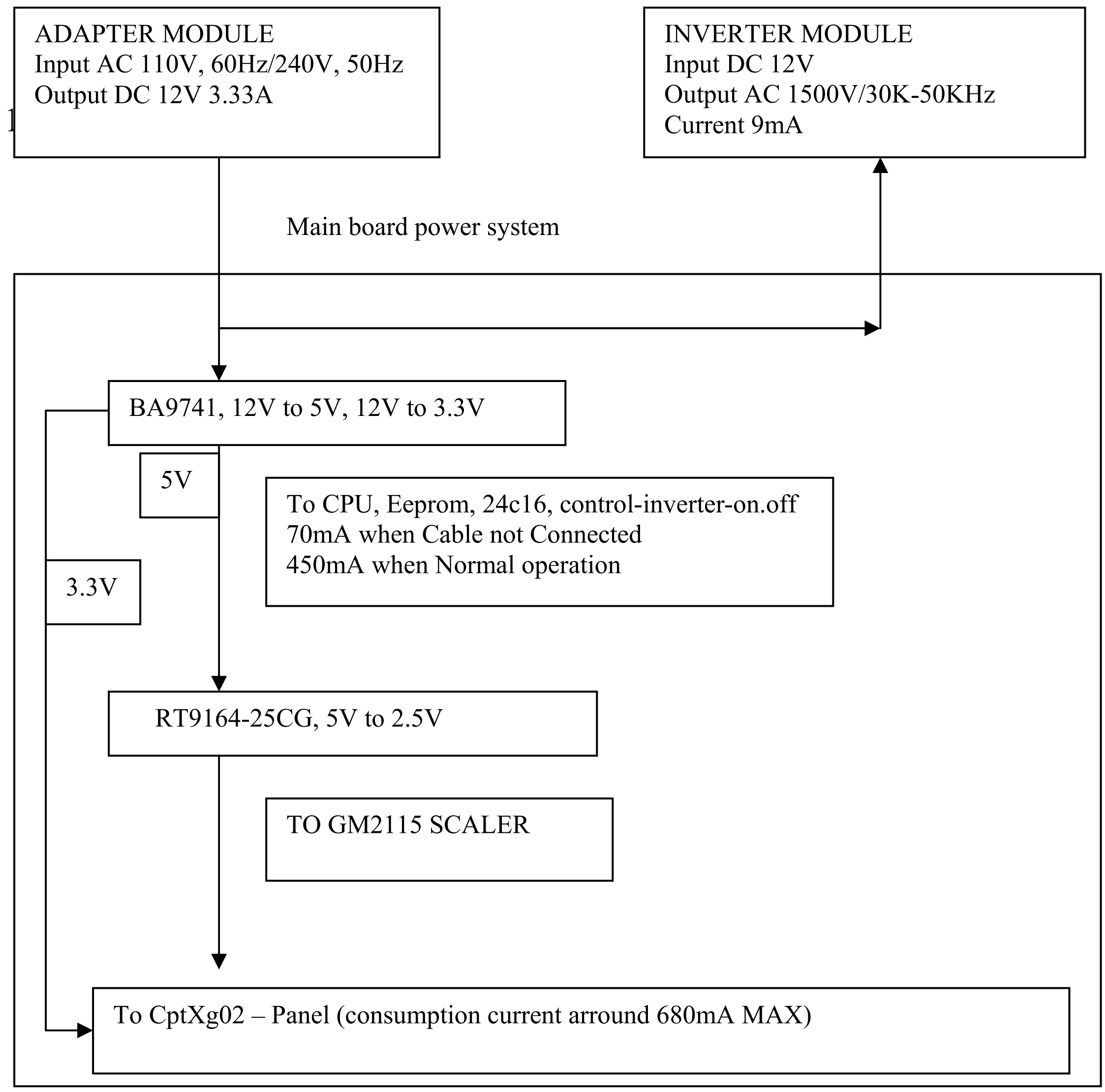
PARTS LIST OF KEY PC BOARD

LOCATION	KEPC560KB3	SPECIFICATION
	AIK560KB3	KEY BOARD FOR T563K*CPQ
VR1	75L 35850322B	VR 50KB CRAY
SW1	77L 600 1GHJ	KEY SWITCH
SW2	77L 600 1GHJ	KEY SWITCH
SW3	77L 600 1GHJ	KEY SWITCH
SW4	77L 600 1GHJ	KEY SWITCH
D1	81L 12 1 BH	3 PIN LED
LN4	88L 302 4C	PHONE JACK
LN4	88L 302 4S	3.5MM EAR PHONE JACK
CN2	95L8014 4 2	HARNESS
CN3	95L8014 5 13	HARNESS
CN1	95L8014 7 2	HARNESS

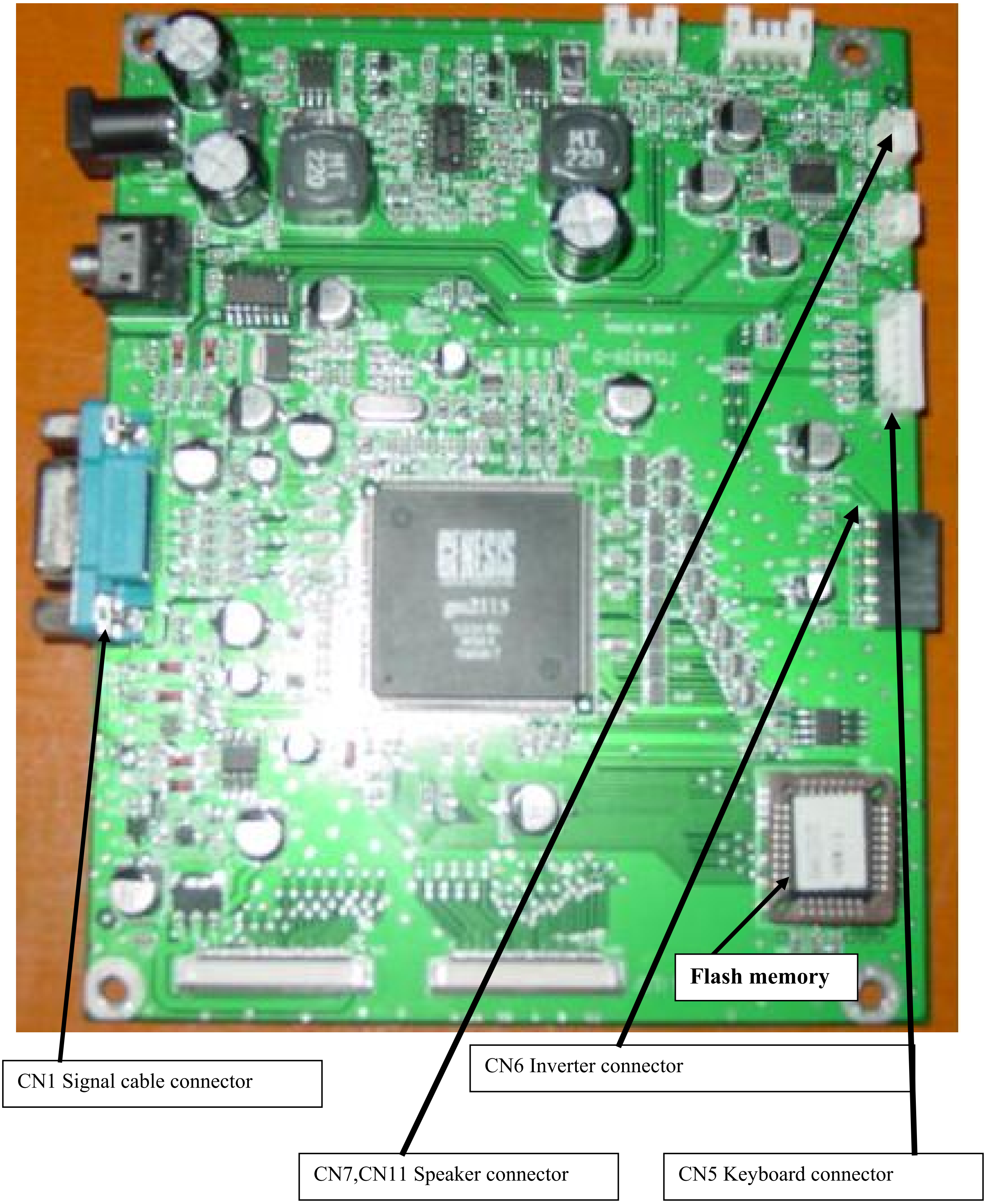
PARTS LIST OF KEY PC BOARD AUTO INSERTION

LOCATION	AIK560KB3	SPECIFICATION
	715L 936 1	LCD 17" KEY BRD + SP
J1	95L 90 23	TIN COATED
J3	95L 90 23	TIN COATED
R1	61L 60233052T	CFR 33 OHM +-5% 1/6W
R2	61L 60233052T	CFR 33 OHM +-5% 1/6W

9. POWER SYSTEM AND CONSUMPTION CURRENT



PCB LAYOUT


Flash memory
CN1 Signal cable connector
CN6 Inverter connector
CN7,CN11 Speaker connector
CN5 Keyboard connector

For Hannstar x82 panel:

AOC gm2115 LCD CONTROLLER BOARD SCHEMATICS

CONTENTS

REVISION HISTORY

Date	Author	Ver	Comments
11/26/01	Jed Huang	A	Preliminary
01/09/02	Eric Chien	B	1.CHANGE PCB DIMENSION FROM 108X139 TO 112X 139 2.CHANGE CN5 FROM 8 PINS TO 7 PINS (STRAIGHT T YPE) 3.SWAP RP6 PIN 1,3 NE T 4.CHANGE CN6 TO 6 PINS FEMALE HEAD ER 5.CHANGE CN7,CN11 TO STRAIGHT TY PE 6.SWAP CN7 PIN 1,2 NE T 7.ADD R74,R75 BETWEEN U8,C N9 8.CHANGE CN10 FROM 6 PINS TO 5 PI NS 9.SWAP CN9,CN10 LOCATIO N 10.DEL F1 11.CHANGE CN5,CN6,CN7,CN9,CN10,CN11 POSIT ION 12.ADD R76,R77 BETWEEN CN1 AND U3 13.CONNECT U3 PIN208 TO NET BAN K0 14.MOVE NET VGA_PG TO U3 PIN1 (GPIO 17) 15.CHANGE C91 PACKAGE FROM 0805 TO 0 603 16.CHANGE U1 PIN 1,2,3 FROM DDC_VCC TO GND
02/06/02 02/27/02	Cheng-Lung	C	1.ADD CAP ARRAY 9 PCS(CP1-CP 9) 1.CHANGE R ARRAY TO BEAD ARRAY(RP2,3,5,7,8,9,10,11 ,12) 2.DEL C78(47uF) 3.ADD L5(T1A55-28) 4.CHANGE CN12(88A304-1S TO 88A304-8 K)
03/13/02		D	1.CHANGE R34 FROM 10K TO N C 2.CHANGE R3,R4 FROM 47K TO 1 0K 3.ADD 1000pF CAP (C62,C105,C106,C107,C108,C109,C110,C117,C121,C122,C 125) 4.ADD 100pF CAP (C103,C104,C111,C112,C113,C11 4, C115,C116,C118,C119,C126,C12 7) 5.CHANGE R46,R51 FROM 20K TO 3 9K 6.ADD NC CAP (C120,C123,C12 4) 7.ADD CAP ARRAY (CP10) NEAR R P1

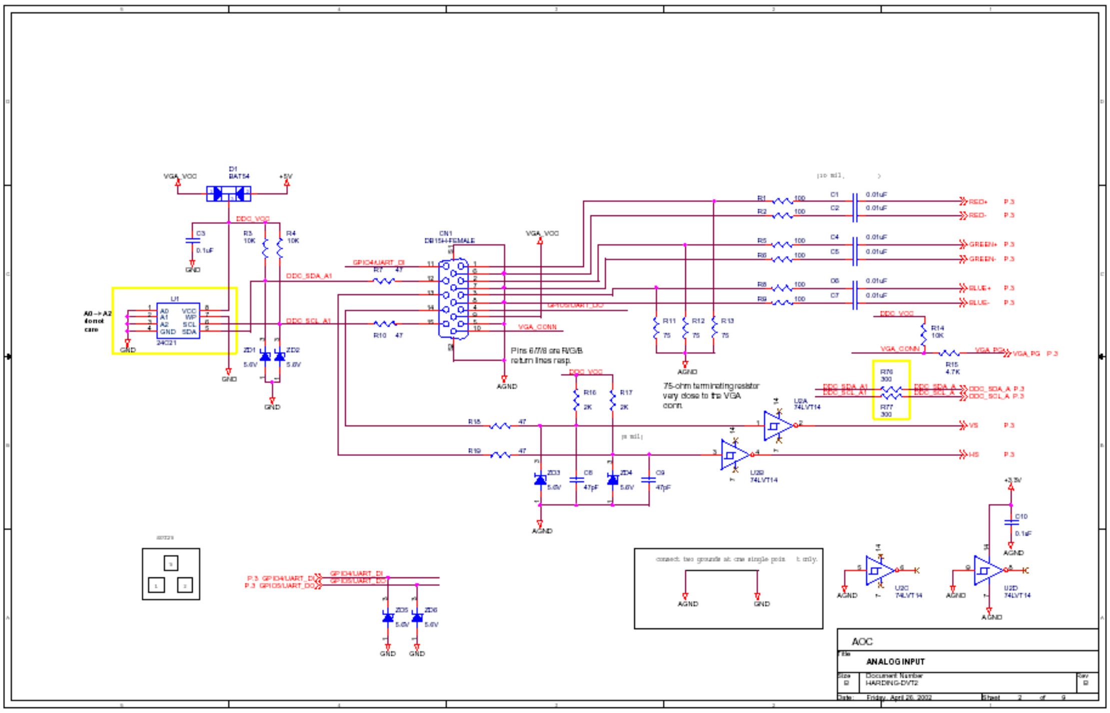
Approval	Organization	Signature	Date

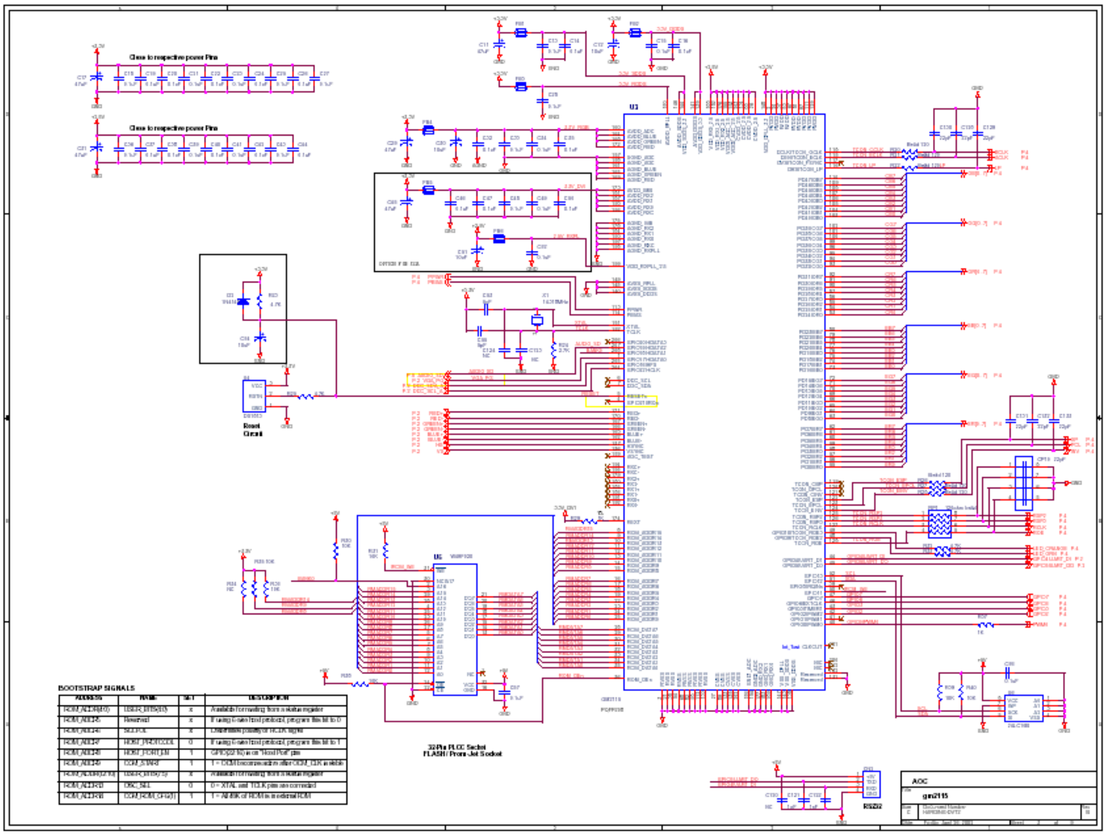
AOC

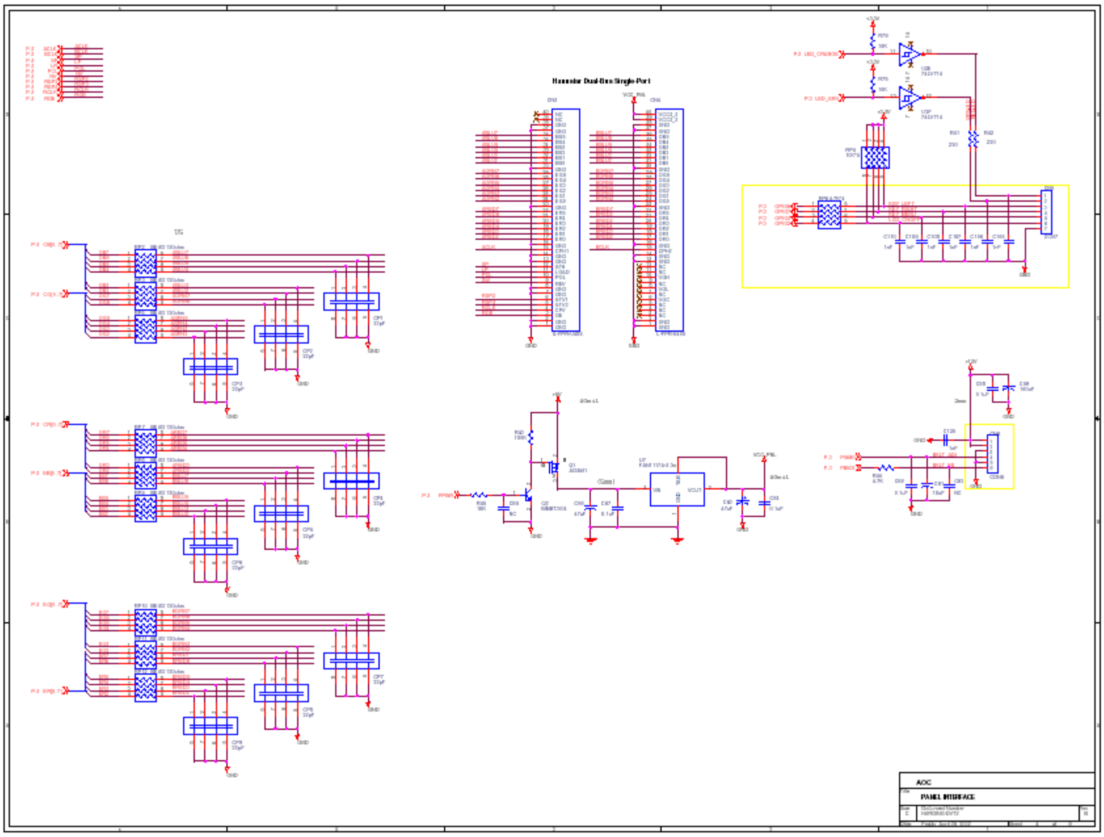
Title: CONTENTS

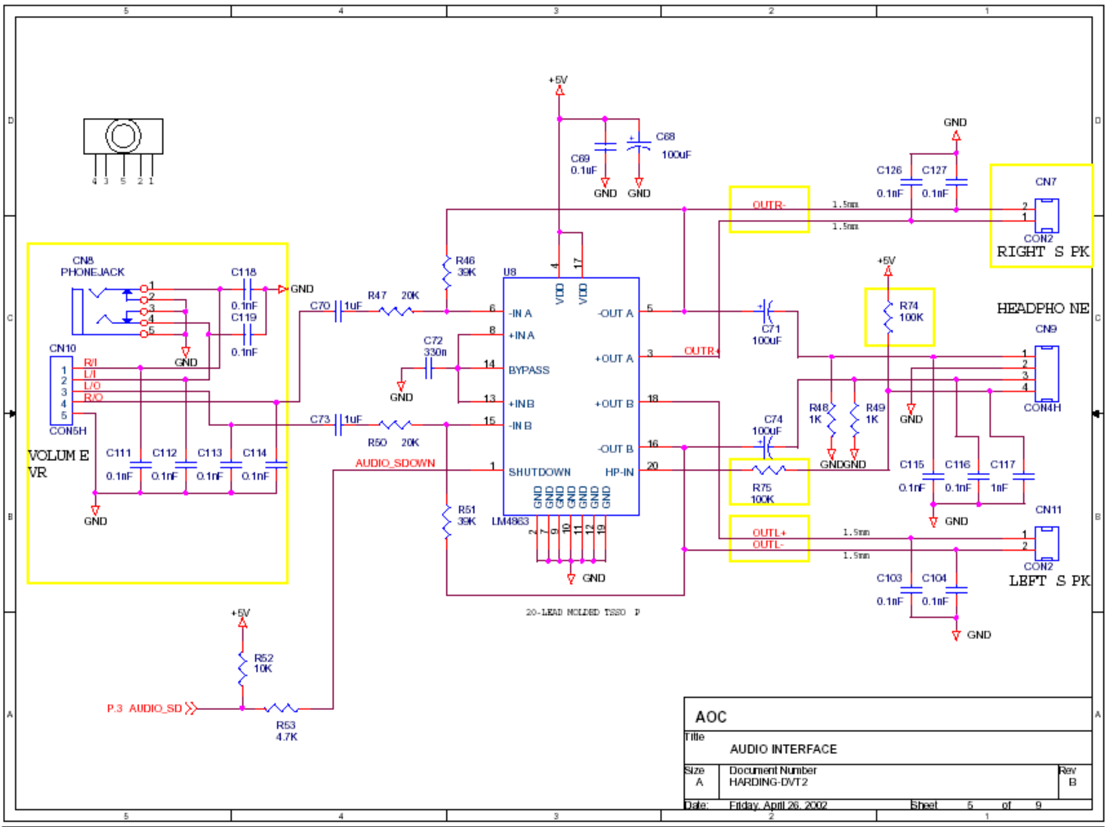
Size	Document Number	Rev
A	HARDING-DVT2	B

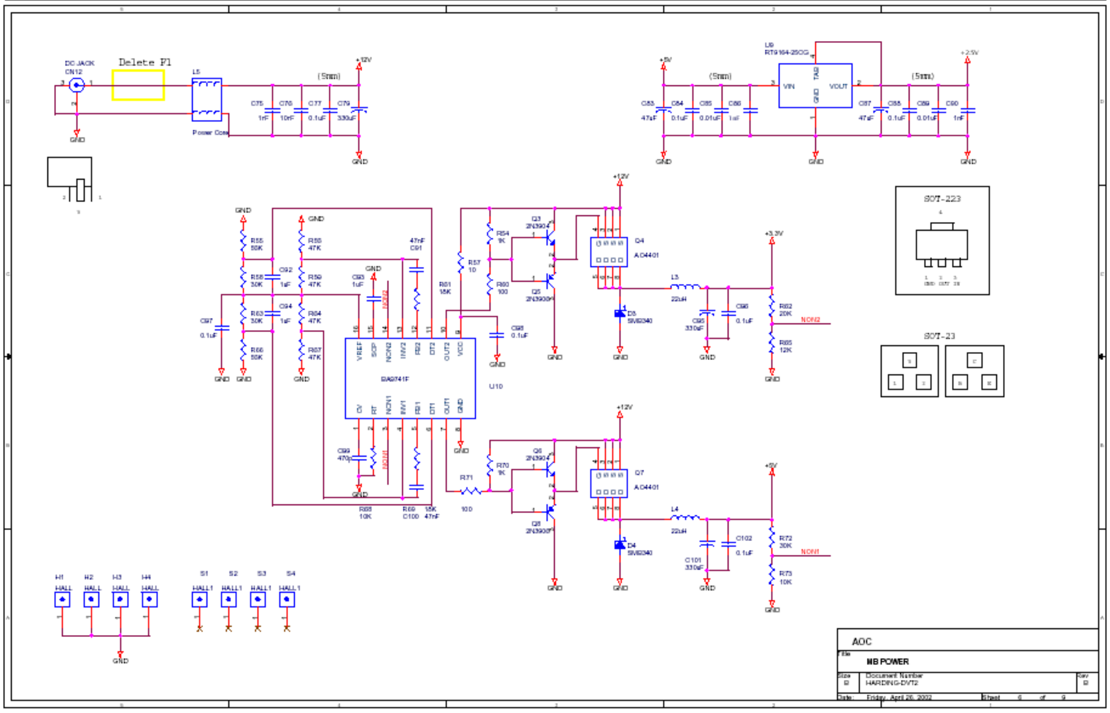
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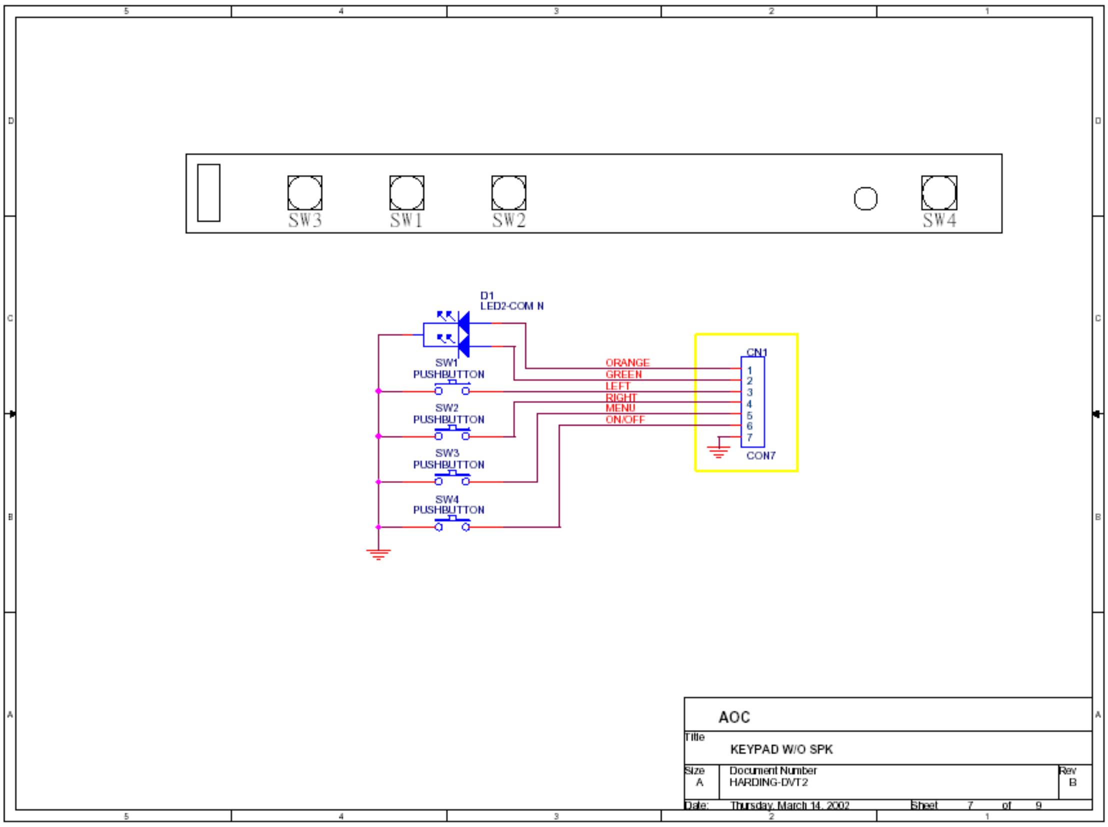


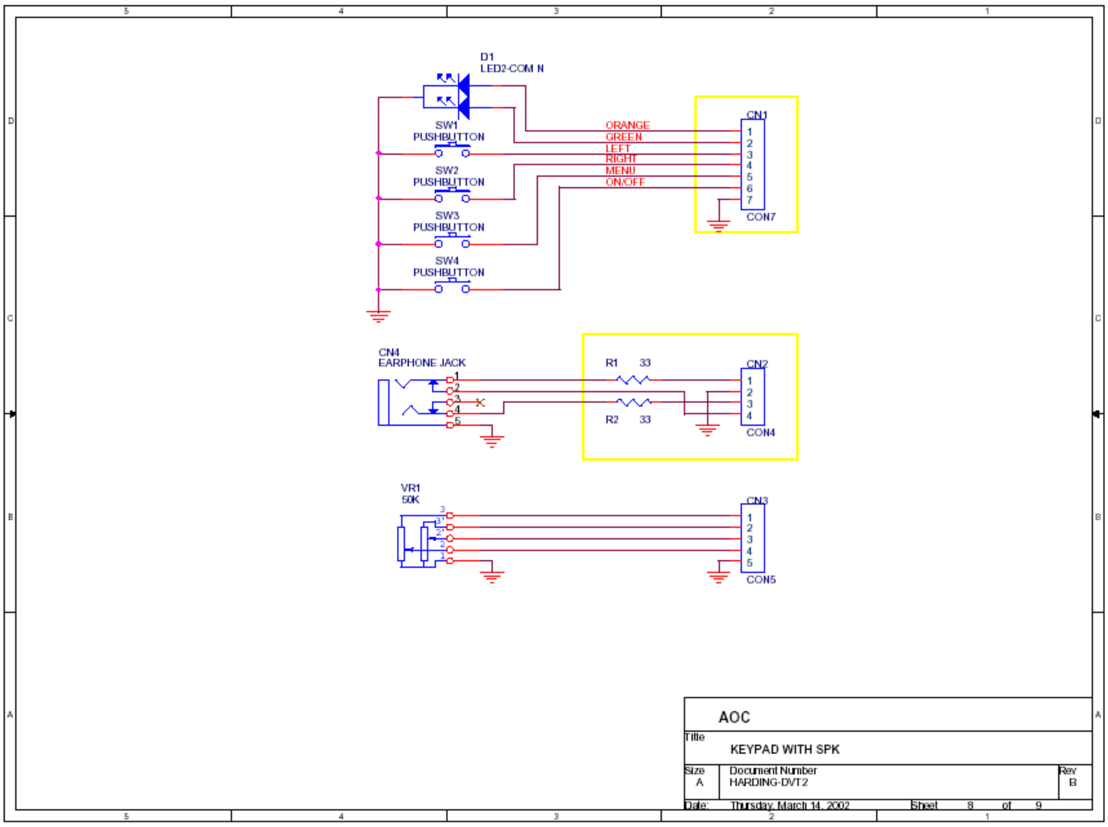

BOOTSTRAP SIGNALS
AOC
gm2115
32 Pin PLCC Socket
FLASH / Prom Jet Socket


AOC
PANEL INTERFACE

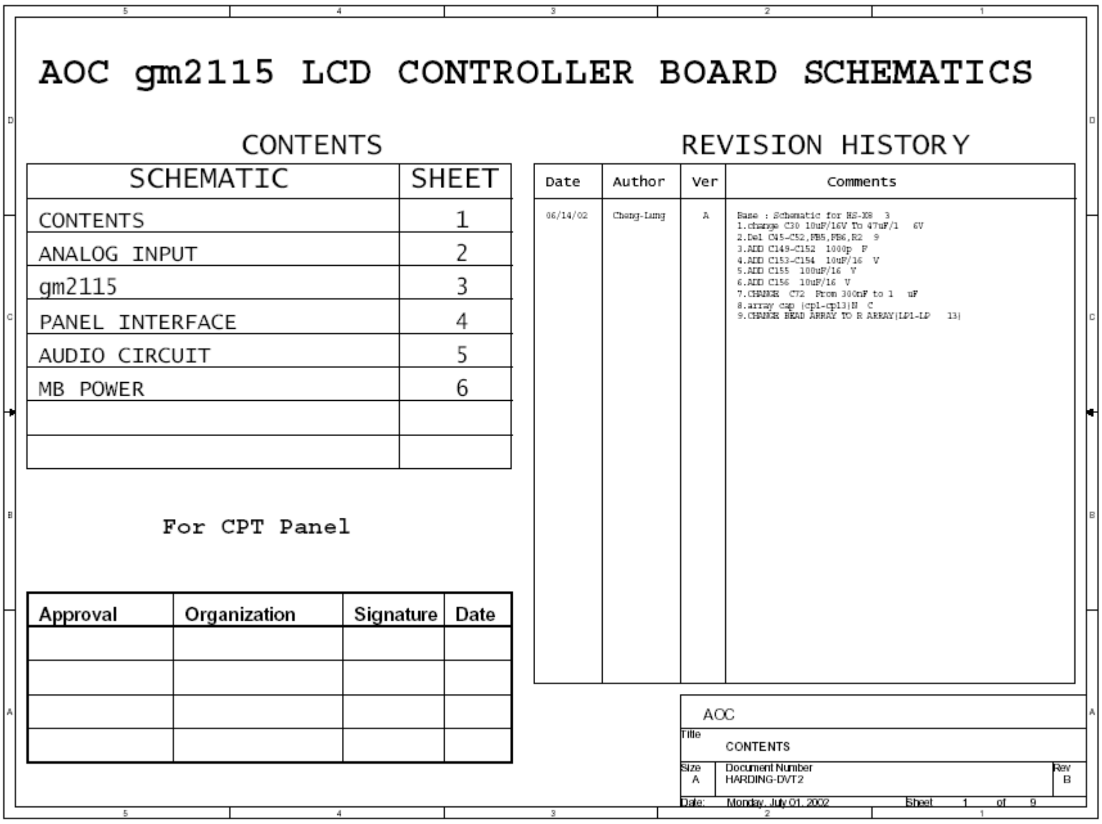

AOC
Title
AUDIO INTERFACE
Size
A
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B
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CN8
PHONEJACK
CN10
CON5H
VOLUM E
VR
CN7
CON2
RIGHT S PK
HEADPHO NE
CN9
CON4H
CN11
CON2
LEFT S PK
U8
LM4863
20-LEAD MOLDED TSSO P
SHUTDOWN
BYPASS
AUDIO_SDOWN
P.3 AUDIO_SD
OUTR-
OUTR+
OUTL+
OUTL-
+5V
GND


AOC
MB POWER
HARDING-DVT2
Delete F1
DC JACK
CN12
SOT-223
SOT-23
BA9741F
U10
+12V
+5V
+3.3V
+2.5V
GND


SW3
SW1
SW2
SW4
D1
LED2-COM N
SW1
PUSHBUTTON
SW2
PUSHBUTTON
SW3
PUSHBUTTON
SW4
PUSHBUTTON
ORANGE
GREEN
LEFT
RIGHT
MENU
ON/OFF
CN1
CON7
AOC
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KEYPAD W/O SPK
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D1
LED2-COM N
SW1
PUSHBUTTON
SW2
PUSHBUTTON
SW3
PUSHBUTTON
SW4
PUSHBUTTON
ORANGE
GREEN
LEFT
RIGHT
MENU
ON/OFF
CN1
CON7
CN4
EARPHONE JACK
R1 33
R2 33
CN2
CON4
VR1
50K
CN3
CON5
AOC
Title
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For CPT XG02 pannel:



AOC gm2115 LCD CONTROLLER BOARD SCHEMATICS

CONTENTS

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gm2115	3
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AUDIO CIRCUIT	5
MB POWER	6

REVISION HISTORY

Date	Author	Ver	Comments
06/14/02	Cheng-Lung	A	Base : Schematic for HS-X8 3 1.change C30 10uF/16V To 47uF/1 6V 2.Del C45-C52,FB5,FB6,R2 9 3.ADD C149-C152 1000p F 4.ADD C153-C154 10uF/16 V 5.ADD C155 100uF/16 V 6.ADD C156 10uF/16 V 7.CHANGE C72 From 300nF to 1 uF 8.array cap (cp1-cp13)N C 9.CHANGE BEAD ARRAY TO R ARRAY(LP1-LP 13)

For CPT Panel

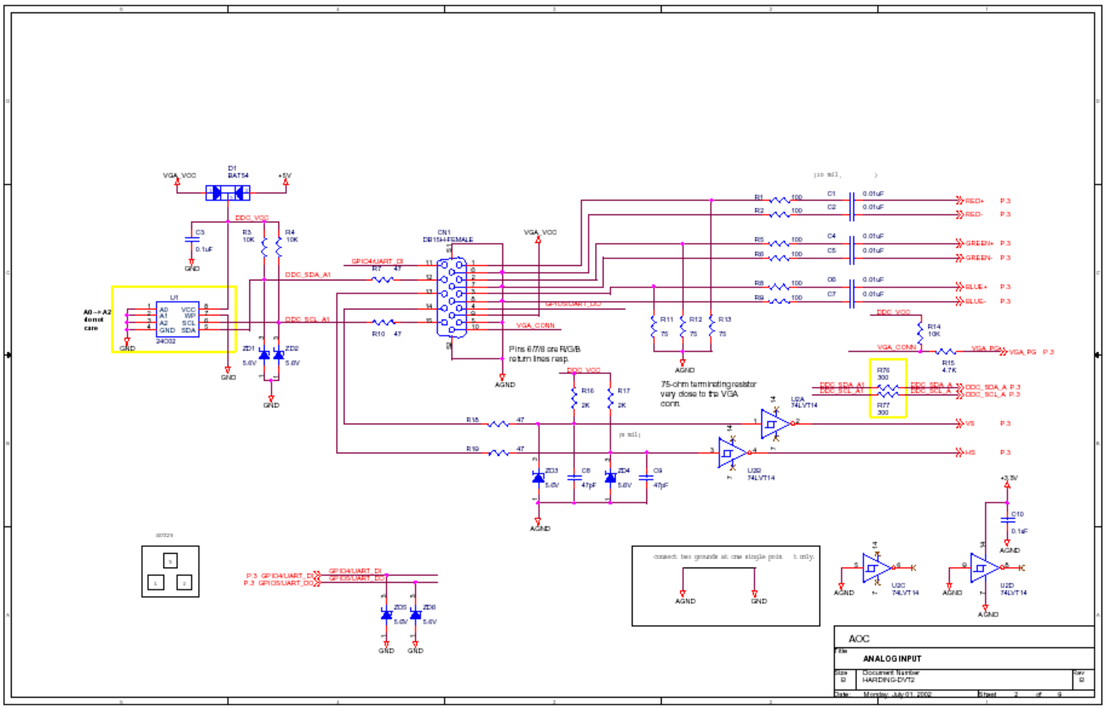
Approval	Organization	Signature	Date

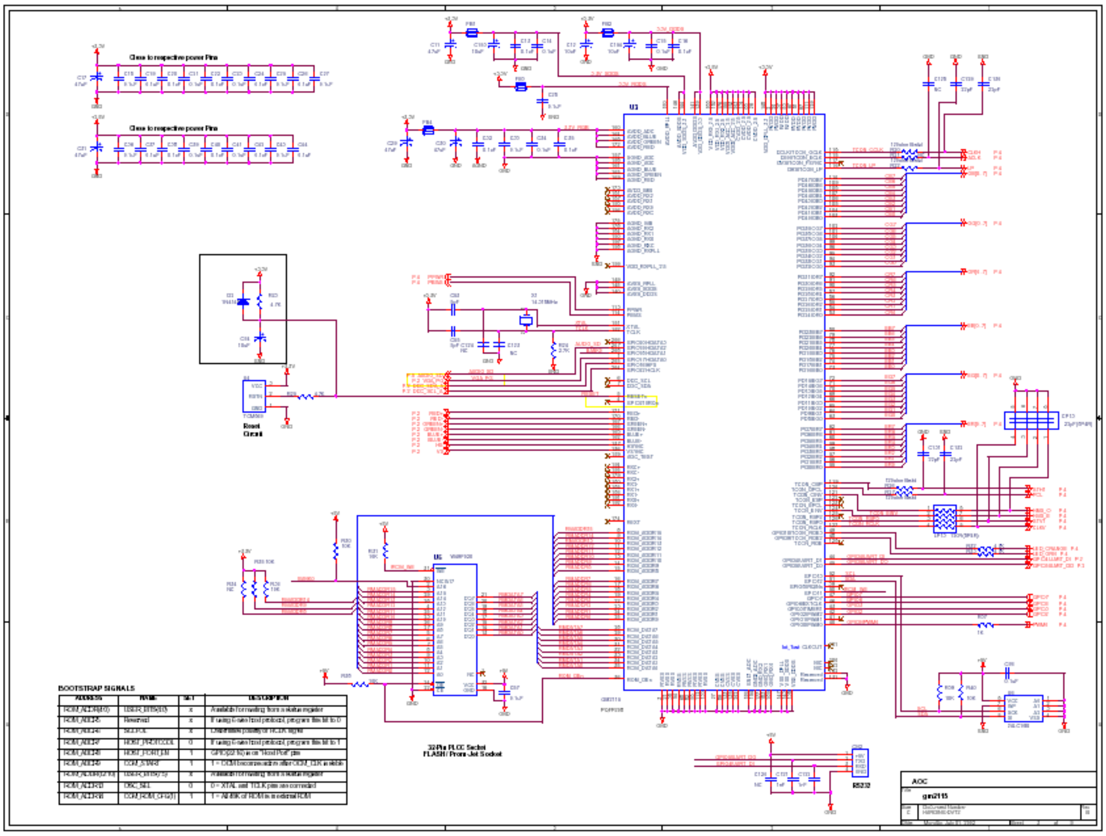
AOC

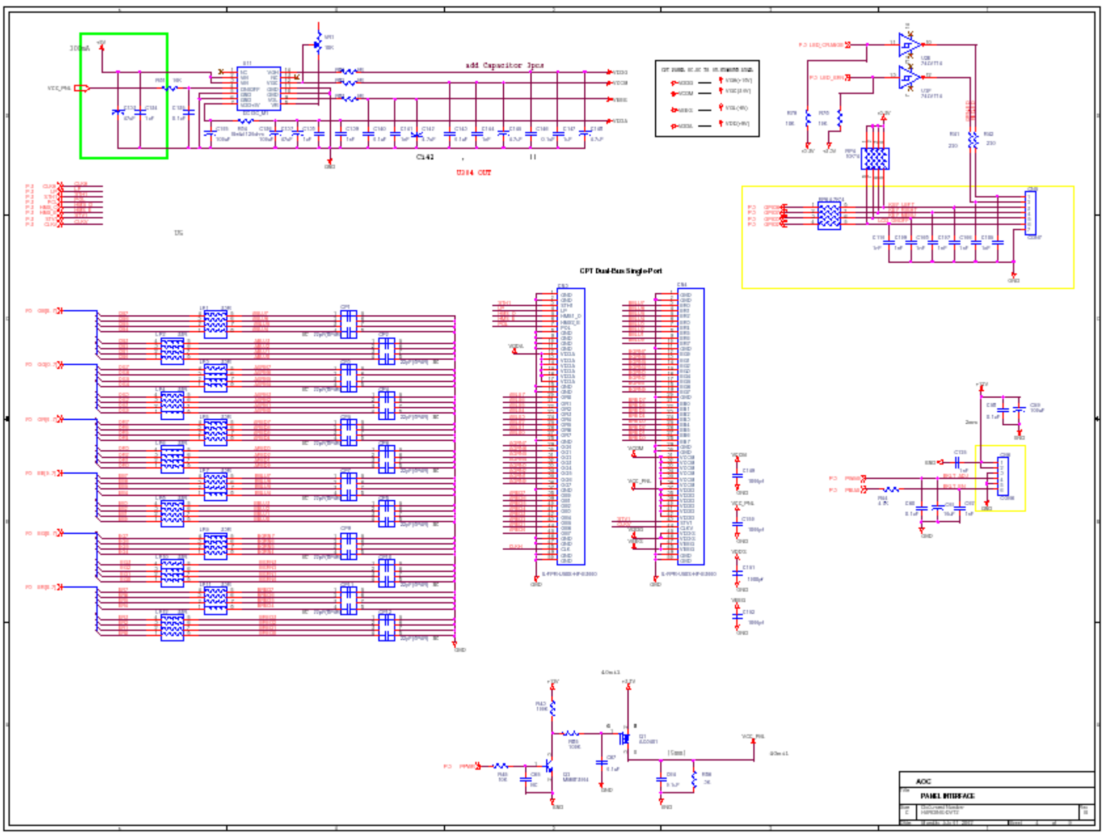
Title: CONTENTS

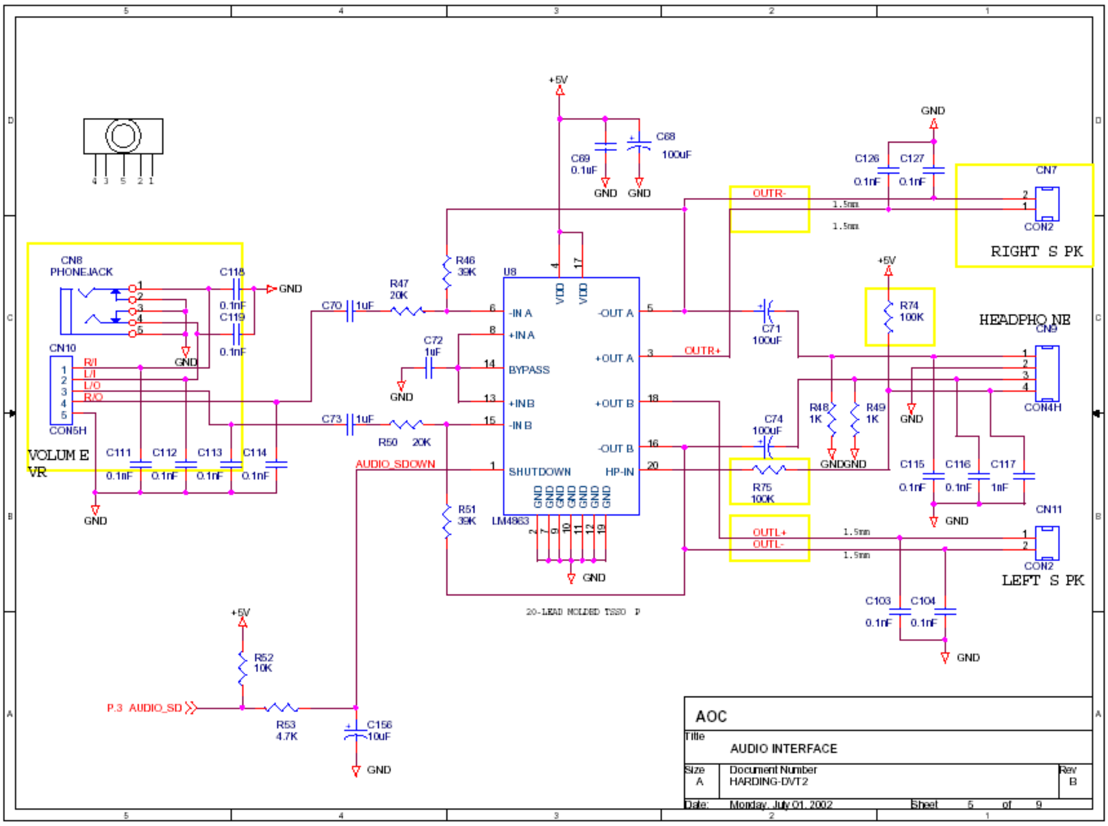
Size: A | Document Number: HARDING-DVT2 | Rev: B

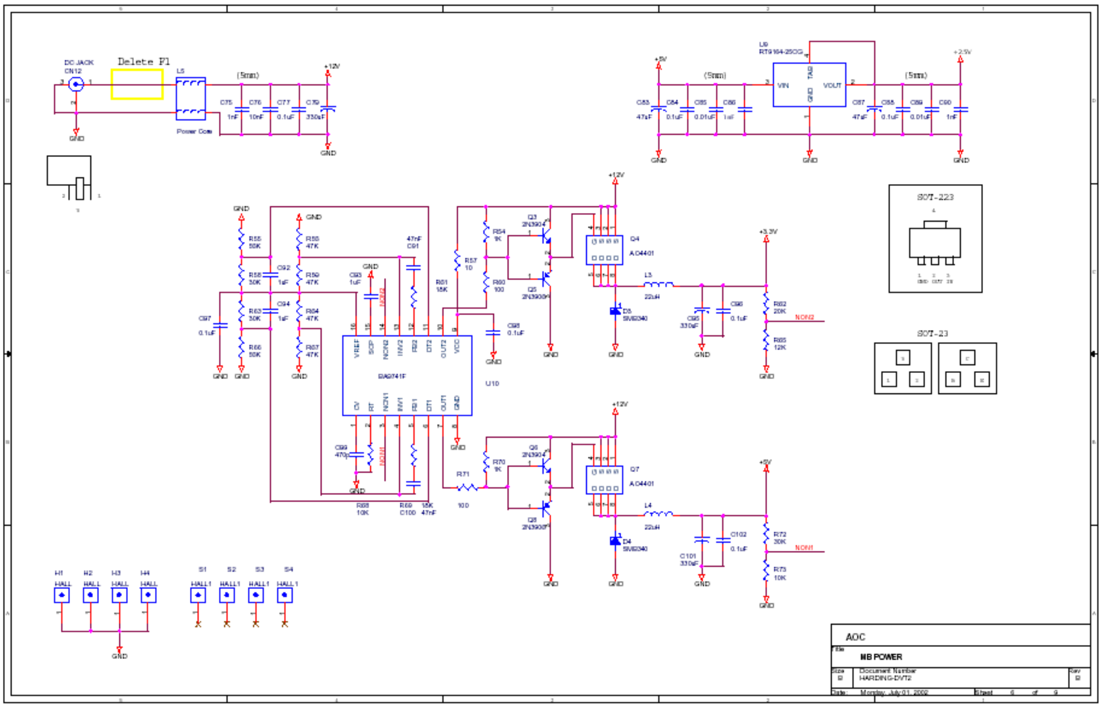
Date: Monday, July 01, 2002 | Sheet 1 of 9

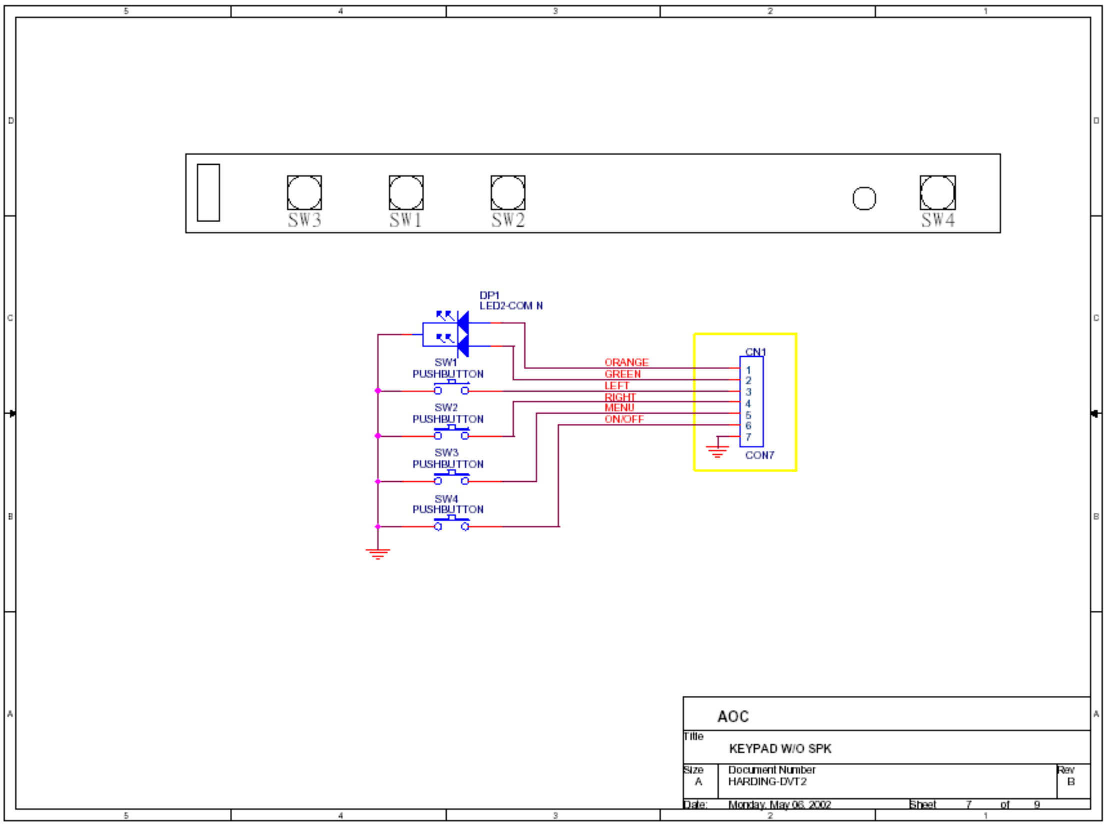


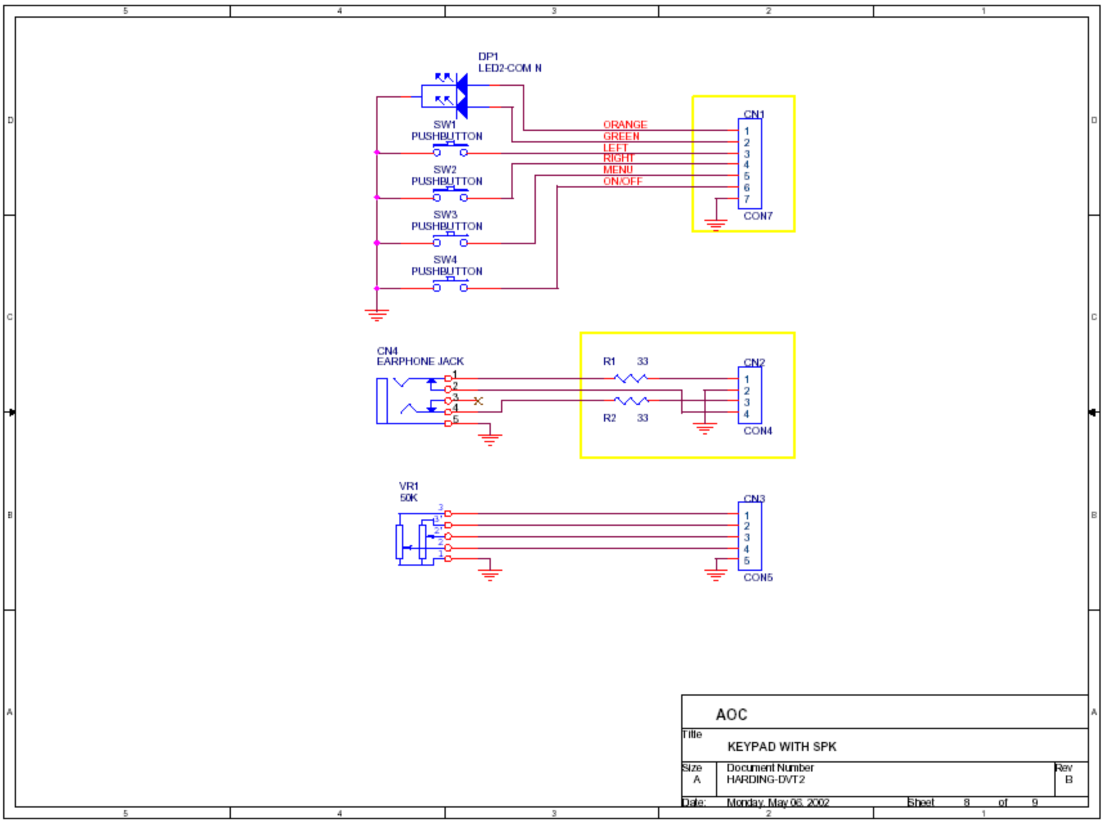

BOOTSTRAP SIGNALS
AOC


CPT Dual-Bus Single-Port
AOC
PANEL INTERFACE


AUDIO INTERFACE
HARDING-DVT2
LM4863
RIGHT S PK
LEFT S PK
HEADPHO NE
VOLUM E VR
AOC


MB POWER
HARDING-DVT2
AOC


SW3
SW1
SW2
SW4
DP1
LED2-COM N
SW1
PUSHBUTTON
SW2
PUSHBUTTON
SW3
PUSHBUTTON
SW4
PUSHBUTTON
ORANGE
GREEN
LEFT
RIGHT
MENU
ON/OFF
CN1
1
2
3
4
5
6
7
CON7
AOC
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DP1
LED2-COM N
SW1
PUSHBUTTON
SW2
PUSHBUTTON
SW3
PUSHBUTTON
SW4
PUSHBUTTON
ORANGE
GREEN
LEFT
RIGHT
MENU
ON/OFF
CN1
1
2
3
4
5
6
7
CON7
CN4
EARPHONE JACK
R1 33
R2 33
CN2
1
2
3
4
CON4
VR1
50K
CN3
1
2
3
4
5
CON5
AOC
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KEYPAD WITH SPK
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